L57 ANSWER 1 OF 20 HCAPLUS COPYRIGHT 2003 ACS
AN 2003:281888 HCAPLUS
DN 138:279781
TI Method of forming reliable interconnects in semiconductor **integrated circuits**
IN Ishikawa, Kensuke; Saito, Tatsuyuki; Miyauchi, Masanori; Saito, Toshio; Ashihara, Hiroshi
PA Japan
SO U.S. Pat. Appl. Publ., 52 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2003067079	A1	20030410	US 2002-263829	20021004
	JP 2003115535	A2	20030418	JP 2001-309007	20011004
PRAI	JP 2001-309007	A	20011004		

AB The invention relates to a method of forming reliable interconnects in semiconductor **integrated circuits** by optimizing the structure of the barrier film. The method involves steps of (i) forming an interconnect trench and a contact hole in an interlayer insulating film formed over a first-level interconnect on a semiconductor substrate; (ii) forming a barrier film inside of the trench and hole so that its film thickness increases from the center of the bottom of the hole toward the sidewalls all around the bottom of the contact hole; (iii) forming a **copper film** over the barrier film; (iv) and forming the second-level interconnect and a connector portion (plug) by chem.-mech. polishing (CMP). The circuit design provides that the geometrically shortest pathway of an elec. current flowing from the second-level interconnect toward the first-level interconnect through a connector portion (plug) does not coincide with a thin barrier film portion which has the lowest **elec. resistance** so that a current pathway can be dispersed and concn. of electrons does not occur readily.

L57 ANSWER 2 OF 20 HCAPLUS COPYRIGHT 2003 ACS
AN 2003:17782 HCAPLUS
DN 138:82113
TI Method for the chemical-mechanical polishing of metal-filled trenches and vias in **integrated circuit** structures
IN Nagahara, Ronald J.; Xie, James J.; Ueno, Akihisa; Pallinti, Jayanthi
PA LSI Logic Corporation, USA
SO U.S., 15 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6503828	B1	20030107	US 2001-882124	20010614
PRAI	US 2001-882124		20010614		

AB The invention relates to a method for the chem.-mech. polishing of metal-filled trenches and vias in **integrated circuit** structures. The **integrated circuit** structure contains (i) one or more openings in a layer of dielec. material; (ii) a main **elec. conductive** layer; and (iii) a diffusion barrier layer lying adjacent to layer of dielec. material, where the diffusion barrier layer and said main **elec. conductive** layer fill one or more openings such that the depressed regions of the main **elec. conductive** layer overlie the openings. The

process consists of the steps of (i) using a photoresist mask and etching process, forming, over depressed regions of the main **elec.** **conductive** layer, a polishing barrier layer selected from the group consisting of silicon carbide, **silicon nitride**, **silicon oxynitride**, tantalum, tantalum nitride, titanium, and titanium nitride; (ii) polishing the portion of the main **elec.** **conductive** layer not covered by the polishing barrier layer; and (iii) then, in a second polishing step, removing portions of the diffusion barrier layer overlying the upper surface of the dielec. layer.

RE.CNT 41 THERE ARE 41 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L57 ANSWER 3 OF 20 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:770170 HCAPLUS
DN 137:287524
TI Semiconductor **chip** substrate coated with a dielectric layer and alloy diffusion barrier for **integrated-circuit** interconnects
IN Wang, Pin-Chin Connie; Marathe, Amit P.; Ngo, Minh Van; Pangrle, Suzette K.
PA Advanced Micro Devices, Inc., USA
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6462417	B1	20021008	US 2001-772750	20010129
PRAI	US 2000-256411P	P	20001218		

AB The **integrated circuit** is manufd. with a semiconductor substrate having semiconductor devices and the assocd. dielec. layer with a channel opening. The alloy layer deposited in the opening contains a metal capable of reacting during thermal treatment with both the conductor core and the channel dielec. layer, to form the alloy barrier to diffusion from the conductor core to the channel dielec. layer. The barrier alloy contains Ti, Ta, and/or W, and is compatible with Cu, Al, Au, and/or Ag as top conductor layer. The typical barrier is based on the **Cu**-Ti alloy **layer** reacting with N in the dielec. base layer to form TiN barrier film, as well as reacting with deposited **Cu** top **layer** for bonding attachment.

RE.CNT 5 THERE ARE 5 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L57 ANSWER 4 OF 20 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:627865 HCAPLUS
DN 137:314204
TI Development of flip **chip** bonding using a substrate with bumps - Application of horizontal ultrasonic vibration
AU Enomoto, Tetsuya; Endo, Toshihiro; Nakamura, Hidehiro; Nakaso, Akishi
CS Interconnection Boards Lab., Res. & Developmetn Center, Hitachi Chemical Co., Ltd., 48 Wadai, Tsukuba-shi, Ibaraki, 300-4247, Japan
SO Symposium on "Microjoining and Assembly Technology in Electronics" (2001), 7th, 157-160
CODEN: SMAEFT
PB Yosetsu Gakkai
DT Journal
LA Japanese
AB From the viewpoint of miniaturization of packages and cost redn. for **chip** mounting, we have examd. the application of horizontal

ultrasonic vibration to flip **chip** bonding of a bumpless **chip** using a substrate with bumps. In this method, adhesive film (Anisotropic Conductive Film (ACF) or Non Conductive Film (NCF)) is temporarily compressed with heating on a substrate with bumps which are formed by stepwise etching process. After the following pattern matching between **chip** and substrate, **chip** bonding is carried out using heat compression and horizontal ultrasonic vibration. Ultrasonic bonding can be accomplished less than 5s and the connection resistance becomes less than 1/4 (about 17 m.OMEGA.) than that in heat compression. From the result of observation and anal. of bonding region, increasing the bonding area and formation of Au-Al intermetallic layer seem to be factors of reducing the resistance.

L57 ANSWER 5 OF 20 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:488196 HCAPLUS
DN 137:55951
TI Method for eliminating reaction between photoresist and spin-on glass
IN Daniels, Brian J.; Dunne, Jude A.; Kennedy, Joseph T.
PA Honeywell International Inc., USA
SO U.S. Pat. Appl. Publ., 40 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002081834	A1	20020627	US 2000-748692	20001226
	WO 2002052642	A2	20020704	WO 2001-US50233	20011220
	WO 2002052642	A3	20030206		

W: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM

RW: GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW, AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR, BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG

	US 2003032274	A1	20030213	US 2002-243528	20020913
PRAI	US 2000-748692	A	20001226		

AB The present invention relates to the formation of structures in **microelectronic** devices such as **integrated circuit** devices. More particularly, the invention relates to the prevention of photoresist poisoning during the formation of **microelectronic** devices. Various layers of conductive metals and dielec. materials are deposited onto a substrate in selective sequence to form an **integrated circuit**. Vias and trenches are formed throughout the structure by exposing and patterning a photoresist material. The dielec. materials of the insulating layers are protected from the photoresist to prevent chem. reactions which lead to photoresist poisoning. This is done by forming a modified surface layer on the dielec. material by either depositing an addnl. layer that covers the dielec. material, or by modifying the exposed surface of the dielec. material to a plasma or chem. treatment.

L57 ANSWER 6 OF 20 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:384964 HCAPLUS
DN 136:378483
TI Dual damascene process for **integrated circuits** that combines low-K dielectric materials and copper
IN Huang, I-Hsiung; Hwang, Jiunn-Ren; Yen, Yeong-Song; Chang, Ching-Hsu

PA United Microelectronics Corp., Taiwan
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6391757	B1	20020521	US 2001-875508	20010606
US 2001-875508		20010606		

PI
PRAI

AB The title dual damascene process involves forming a 1st passivation layer, a 1st dielec. layer and a 2nd passivation layer on a substrate of a semiconductor **wafer**. A 1st lithog. and etching process was performed to form at least one via hole in the 2nd passivation layer and the 1st dielec. layer. Thereafter, a 2nd dielec. layer and a 3rd passivation layer are formed on the surface of the semiconductor **wafer** followed by performing a 2nd lithog. and etching process to form at least one trench in the 3rd passivation layer and the 2nd dielec. layer. The trench and the via hole together construct a dual damascene structure. Finally, a barrier layer and a metal layer are formed on the surface of the semiconductor **wafer**, and a chem.-mech.-polishing (CMP) process was performed to complete the dual damascene process.

RE.CNT 12 THERE ARE 12 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L57 ANSWER 7 OF 20 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:315448 HCAPLUS
DN 136:348601
TI Method of forming fluorinated silica film in manufacturing semiconductor device and film forming apparatus
IN Suzuki, Yoichi; Shimayama, Tsutomu
PA Applied Materials, Inc., Japan
SO U.S. Pat. Appl. Publ., 20 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2002048969	A1	20020425	US 2001-4489	20011023
JP 2002141348	A2	20020517	JP 2000-322849	20001023
JP 2000-322849	A	20001023		

PI
PRAI

AB The present invention provides a deposition method and deposition app. capable of forming a F-contg. Si inorg. insulating film of stable film properties and a method of manufg. a semiconductor device. Deposition app. comprises parallel plate type electrodes arranged within reaction chamber,gas supply sources for feeding process gas contg. SiH4, SiF4 and O source substance into reaction chamber, valves, gas mixing chamber, and power source that supplies RF power for generating the plasma of the process gas. In this deposition app., power source is capable of supplying RF power of .gtoreq.1000 W to parallel plate type electrodes. In this app., fluorine-contg. Si oxide film is deposited on **wafer** by generating the plasma of process gas contg. SiH4, SiF4 and N2O.

L57 ANSWER 8 OF 20 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:151528 HCAPLUS
DN 136:209078
TI Pillar process for multilevel copper interconnect scheme in fabricating **integrated circuits**
IN Tae, Kim Hyun; Ang, Kim Hock; Quek, Kiok Boone Elgin
PA Chartered Semiconductor Manufacturing Ltd., Singapore

SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6350695	B1	20020226	US 2000-594414	20000616
PRAI US 2000-594414		20000616		

AB A method for forming reliable inter-level metal interconnections in semiconductor **integrated circuits** is described where pillars are formed to connect between different metal layers. A 1st conductive layer is deposited overlying a substrate. A conductive etch stop layer is deposited overlying the 1st conductive layer and then patterned to form a mask for the fist conductive layer. This is followed by a deposition of via metal layer overlying the entire surface. A hard mask layer is deposited and patterned to form the mask where via pillars are to be formed. Subsequent anisotropic etching forms pillars in the via met layer and openings in the 1st conductive layer. An inter-metal dielec. (IMD) layer is deposited covering and filling both the openings in the 1st conductive layer and in between the via pillars. The surface is then planarized.
RE.CNT 9 THERE ARE 9 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L57 ANSWER 9 OF 20 HCAPLUS COPYRIGHT 2003 ACS
AN 2001:355102 HCAPLUS
DN 134:347189
TI System and method for bonding over active **integrated circuits**
IN Saran, Mukul
PA Texas Instruments Incorporated, USA
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6232662	B1	20010515	US 1999-347212	19990702
PRAI US 1998-92961P	P	19980714		

AB An architecture and method of fabrication for an **integrated circuit** having a reinforced bond pad comprising .gtoreq.1 portion of the **integrated circuit** disposed under the bond pad; and this .gtoreq.1 circuit portion comprises .gtoreq.1 dielec. layer and a patterned **elec. conductive** reinforcing structure disposed in this .gtoreq.1 dielec. layer.
RE.CNT 2 THERE ARE 2 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L57 ANSWER 10 OF 20 HCAPLUS COPYRIGHT 2003 ACS
AN 2000:879362 HCAPLUS
DN 134:106278
TI On some special features of the structure and properties of metallic "thin" films
AU Bykov, Yu. A.; Karpukhin, S. D.; Gazukina, E. I.
CS N. E. Bauman Moscow State Technical University, Moscow, Russia
SO Metal Science and Heat Treatment (Translation of Metallovedenie i Termicheskaya Obrabotka Metallov) (2000), 42(5-6), 250-252
CODEN: MHTRAN; ISSN: 0026-0673
PB Consultants Bureau

DT Journal
LA English
AB The structure and properties were investigated of thin **films** of **Cu**, Al, and Ni to be used in **microelectronics** applications as **elec. conductors**. Thin films of nanosize thickness differed substantially from massive films in their elec. resistivity as the resistivity of thin films is detd. by the thickness so that it can exceed that of the metals themselves by an order of magnitude or more when the thickness is decreased. In some cases, the thin films behaved like dielecs.; i.e. they were optically transparent and broke under the action of an elec. current by the mechanism of surface and thermal breakdowns. The voltage of the surface breakdown and the fracture behavior of the metallic films depended on the elec. resistivity of the material and the size of the crystallites in the surface layer of the film. The smaller the crystallites and the higher the elec. resistivity, the higher the breakdown voltage.
RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L57 ANSWER 11 OF 20 HCAPLUS COPYRIGHT 2003 ACS
AN 1997:372354 HCAPLUS
DN 127:115381
TI V2O5 and .beta.-CuxV2O5 thin films grown by MOCVD
AU Gleizes, A.; Bufforn, J. M.; Salzman, C.; Virette, E.; Senocq, F.
CS Lab. "Cristallochim., React. Protection Materiaux", E.N.S. Chim. Toulouse (I.N.P.T.), Toulouse, F-31077, Fr.
SO Materials Research Society Symposium Proceedings (1997), 453(Solid-State Chemistry of Inorganic Materials), 77-82
CODEN: MRSPDH; ISSN: 0272-9172
PB Materials Research Society
DT Journal
LA English
AB Thin films of V2O5 and .beta.-CuxV2O5 were grown by MOCVD using VO(O-iso-Pr)3 and Cu(tmhd)2 (tmhd = tetramethylheptanedionato) as precursor mols. Films were grown on **chips** of Si3N4 coated Si **wafers** in a cold wall reactor using a H.F. heater. A mixt. of He and O was used as a reactive carrier gas, and depositions were performed at low pressure. The films were examd. by SEM, characterized by XRD, and analyzed by EDS and EMPA techniques. All the films proved to be C free. For V2O5, the substrate temp. was varied from 450 to 630.degree.. The films are highly c-axis oriented for both ends of the temp. range, and less oriented for intermediate temps. For 630.degree., the XRD pattern consists almost entirely of reflections (001) and (002). For .beta.-CuxV2O5, the substrate temp. was varied from 450.degree. to 650.degree.. Pure .beta.-phase films with x varying from 0.25 to 0.55 were obtained at >500.degree., by using well chosen gas phase compn. Morphol. and texture depend dramatically on the temp. The most oriented films exhibit a strong anisotropy of surface **elec. cond**
.

L57 ANSWER 12 OF 20 HCAPLUS COPYRIGHT 2003 ACS
AN 1995:14764 HCAPLUS
DN 122:11677
TI Conductive adhesives as **die**-bonding materials for power electric modules
AU Lenkkeri, Jaakko; Rusanen, Outi
CS Electron. Lab., VTT Tech. Res. Cent. Finland, Oulu, Finland
SO Journal of Electronics Manufacturing (1993), 3(4), 199-204
CODEN: JELMEK; ISSN: 0960-3131
DT Journal
LA English

AB Five epoxy-based silver-filled adhesives have been tested with respect to their usefulness for **die**-bonding of power **chip** components. The **elec. resistance** and mech. strength are tested at high temp. aging and high temp./high humidity aging. Test structures contain copper plates with either nickel or Au/Ni plating joined to thick **films** of AgPt, **Cu** or Au on alumina substrate. In accelerated aging tests the structures with Au/Ni-plated surfaces gave better results than those with Ni plating. Of the 5 adhesives only one showed good results for all the metal films. The thermal resistance is measured for silicon diodes either glued or soldered on alumina substrate. The results agree fairly well with those estd. by thermal simulations.

L57 ANSWER 13 OF 20 HCAPLUS COPYRIGHT 2003 ACS
AN 1994:149965 HCAPLUS
DN 120:149965
TI Characterization of thin titanium oxide adhesion layers on gold: resistivity, morphology, and composition
AU Vogt, K. W.; Kohl, P. A.; Carter, W. B.; Bell, R. A.; Bottomley, L. A.
CS Georgia Institute of Technology, Atlanta, GA, 30332-0100, USA
SO Surface Science (1994), 301(1-3), 203-13
CODEN: SUSCAS; ISSN: 0039-6028
DT Journal
LA English
AB Group 1B **metal films** (**copper**, silver and gold) are attractive for metalizations in multichip modules (MCM) and **integrated circuits** because they have high **elec. conductivities**. Unfortunately, Group 1B metals require addnl. bonding layers for adhesion to insulators (i.e. silicon dioxide or polymers). In this work, thin elec. insulating films of titanium oxide on titanium were investigated as adhesion layers between gold and a wide variety of insulators. The adhesion layer does not alter the dielec. properties of the insulator surrounding the metal because it is thin. The morphol., compn., and resistivity of the titanium oxide films were studied with angle resolved XPS, scanning tunneling microscopy, and **elec. resistance** measurements. The results show that sputter-deposited titanium films grow by an island growth (Volmer-Weber) mechanism. The islands coalesce after 10-20 .ANG. of titanium deposition. Following deposition, the titanium films were oxidized by exposure to air at relatively low temps. (T<100.degree.C). Very thin titanium films (3 .ANG.) oxidized completely. When thin titanium films (10-20 .ANG.) were oxidized, a layered film formed with a sub-oxide (TiO) core and a titanium dioxide surface layer. When thicker films (>20 .ANG.) were oxidized, a layered film was also produced with a titanium core and titanium oxide surface layer.

L57 ANSWER 14 OF 20 HCAPLUS COPYRIGHT 2003 ACS
AN 1994:36330 HCAPLUS
DN 120:36330
TI Plastic-supported metal strip manufactured by **wafer** deposition and electroplating
IN St-Amant, Guy; Carignan, Claude
PA Hydro-Quebec, Can.
SO Eur. Pat. Appl., 12 pp.
CODEN: EPXXDW
DT Patent
LA French
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 533575	A1	19930324	EP 1992-402561	19920917

R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LI, LU, MC, NL, PT, SE

	CA 2051604	AA	19930318	CA 1991-2051604	19910917
	JP 05195287	A2	19930803	JP 1992-290660	19920917
	US 5423974	A	19950613	US 1994-314522	19940919
PRAI	CA 1991-2051604		19910917		
	US 1992-945893		19920917		

AB A nonconductive strip is (1) vacuum metalized on .gtoreq.1 side to obtain an **elec. conductive** surface and (2) electroplated with .gtoreq.1 metal to obtain an adherent metal layer 0.1-4 .mu.m thick. Typically, a polymer substrate is polypropylene, polyethylene, polyester, polysulfone, or polyimide. Metalization is done with Cu, Au, Ag, Fe, Ni, Cr, Zn, Mo, or their alloys to obtain a surface **elec. resistance** of 0.1-10 .OMEGA./square. Electroplating is done with Cu, Ni, Fe, Mo, Au, Ag, Cr, Zn, Pb, Cd, or their alloys. The metalized plastic strips are suitable as current collectors for Li batteries with a polymer electrolyte, packaging material permeable to gases and humidity, flexible **elec. conductors**, and light shields. Thus, a polypropylene strip was vacuum **metalized** with **Cu** to obtain a surface with **elec. resistance** of 0.5 .OMEGA./square, and electroplated with Ni at a c.d. of 0.05-0.3 A/cm2 to obtain a Ni layer 0.3 .mu.m thick with **elec. resistance** of 0.15 .OMEGA./square.

L57 ANSWER 15 OF 20 HCAPLUS COPYRIGHT 2003 ACS
AN 1985:543112 HCAPLUS
DN 103:143112
TI Electric conductive adhesive films for fixing semiconductor devices
PA Nitto Electric Industrial Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 60102750	A2	19850606	JP 1983-212652	19831109
	JP 06036416	B4	19940511		
PRAI	JP 1983-212652		19831109		

AB **Die** bonding adhesive films are prepd. by coating an **elec. conductive** film on both sides with mixts. of thermoplastic resins (m.p. 170-320.degree.) and **elec. conductive** fillers. The difference of the m.p. of the thermoplastic resins on the 2 sides is .gtoreq.15.degree.. Thus, a 20-.mu. polyimide film was coated on one side with a mixt. of CF2:CFCF3-CF2:CF2 copolymer (I) [25067-11-2] [m.p. 270.degree., decompn. temp. (Td) 419.degree.] and 4% carbon to thickness 10 .mu. and on the other side with a mixt. of perfluorovinyl ether-CF2:CF2 copolymer (II) [57578-63-9] (m.p. 305.degree., Td 464.degree.) and 4% carbon to thickness 10 .mu., pressed with a Si **wafer** on the I side, and pressed with a 42 Alloy plate on the II side at 5 kg/cm2 and 350.degree. for 5 s to give a product with shear adhesive strength at 200.degree. 20 kg/cm2 and **elec. resistance** 100 .OMEGA..

L57 ANSWER 16 OF 20 HCAPLUS COPYRIGHT 2003 ACS
AN 1981:35175 HCAPLUS
DN 94:35175
TI Wire forming process for copper-cored titanium wire
IN Brendel, Thomas A.; Turillon, Pierre P.
PA International Nickel Co., Inc., USA
SO U.S., 4 pp.
CODEN: USXXAM

DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 4224085	A	19800923	US 1978-926754	19780721
PRAI	US 1978-926754		19780721		

AB Ti-clad Cu-cored wire of <16 gage with corrosion resistance and improved **elec. cond.** is made by cold drawing a Ti tube filled with Cu powder in several passes at initial-to-final **die** size ratio 10-500, preferably .apprx.100. The heat treatment for annealing is at 540-870.degree. for 0.1-4 h, preferably 815.degree. for 1 h. Thus, com.-grade Ti tubing, 12.7 mm outside diam. and 0.85 mm wall thickness was filled with com. Cu powder (.gtoreq.99.25%) of particle size < 200 mesh, swaged to seal the ends, heated 1 h at 815.degree., cold-drawn to 5.8 mm diam., annealed at 815.degree., cold-drawn to 1.73, final-annealed, and cold-drawn to final wire size of 1.02 mm outside diam., at 10-18% redn./pass. The wire had a continuous crack-free surface of .apprx.0.04 mm thick Ti cladding with a solid Cu core of >98% d., **elec. resistance** 0.1084 .OMEGA. at 2.13 m length, and was useful for **elec. conductors** or electrodes in corrosive environments including molten glass and silicates, for electrochem. app. and implants, for cathodic protection electrodes in marine environment, and wire gages in corrosive industrial atms. The as-drawn wire had tensile and yield strength 48.3 and 47.7 H bar, resp., elongation 0.3%, and satisfactory ductility for bending completely around a 0.32 cm diam. rod.

L57 ANSWER 17 OF 20 HCAPLUS COPYRIGHT 2003 ACS
AN 1956:27534 HCAPLUS
DN 50:27534
OREF 50:5498f-i,5499a-i,5500a-g
TI American Society for Testing Materials, Standards, 1955. II. Nonferrous metals
SO (1955), 1480 pp.
DT Book
LA Unavailable
AB Standards or tentative standards, adopted or revised in 1955, are given for: electrodeposited coatings of Zn, Cd, Pb, Ni, and Cr on steel; test for local thickness of electrodeposited coatings; descaling and cleaning stainless-steel surfaces; hard-drawn, medium-hard-drawn, and soft or annealed Cu wire; lake and electrolytic Cu-wire bars, cakes, slabs, billets, ingots, and ingot bars; slab Zn (spelter); concentric-lay-stranded Cu conductors; bronze trolley wire; Cu plates for locomotive fireboxes; Cu rods for locomotive staybolts; seamless Cu boiler tubes; free-cutting brass rod, bar, and shapes; cartridge-brass sheet, strip, plate, bar, and disks; navalbrass rod, bar, and shapes; bronze castings for bridges and turntables; white metal bearing alloys; Al ingots for remelting; Al-base alloy sand castings; pig lead; Cu-base alloys in ingot form for sand castings; soft solder metal; tinned soft or annealed Cu wire; brass plate, sheet, strip, and rolled bar; Al for use in Fe or steel manuf.; Ni; seamless Cu and red-brass pipe; Cu trolley wire; soft rectangular and square bare Cu wire for **elec. conductors**; hot-rolled Cu rods; phosphor and SiCu; steam or valve bronze castings; compn. brass or ounce metal castings; test for resistivity of metallically conducting resistance and contact materials and of **elec. conductor** materials; bronze castings in the rough for locomotive wearing parts; lined car and tender journal bearings; seamless bright-annealed Cu tube; rolled Zn; test for change of resistance with temp. of metallic materials for elec. heating; fire-refined casting Cu; seamless Cu tube; accelerated life test for metallic materials for elec. heating; test for thermoelec, power of **elec.-resistance**

alloys; Mg-base alloy sand castings; 80% Ni, 20% Cr and 60% Ni, 10% Cr, and balance Fe, drawn or rolled alloys for elec.-heating elements; test for temp.-resistance consts. of alloy wires; Al-base alloy and Zn-base alloy **die** castings; seamless Cu water tube; Mg-base alloy sheet and forgings; Mg ingot and stick for remelting; Mg-base alloys ingot form for sand castings, **die** castings, and permanent mold castings; Mg-base alloy **die** castings; test for linear expansion of **metals**; **Cu**-Si alloy plate and sheet for pressure vessels; Cu-Si alloy plate, sheet, strip, and rolled bar for general purposes; Cu-Si alloy, rod, bar, shapes, and wire; rolled Cu-alloy bearing and expansion plates and sheets; Pb-**coated Cu** sheets; Pb- and Sn-base alloy **die** castings; phosphor bronze plate, sheet, strip, and rolled bar; hard-drawn Cu alloy wires for **elec** . **conductors**; testing thermostar metals; Mg-base alloy bars, rods, and shapes; Al-base alloy permanent mold castings; test for dielec. strength of anodically **coated** Al; **Cu** and Cu-alloy seamless condenser tubes and ferrule stock; test for temp.-resistance consts. of sheet materials; electrolytic cathode Cu; figure-9 deep-section grooved and figure-8 Cu trolley wire; salt spray (fog) testing; classification of cast Cu-base alloys; leaded brass plate, sheet, strip, and rolled bar; Cu-Ni-Zn alloy and Cu-Ni alloy plate, sheet, strip, and rolled bar; Cu and Cu-alloy forging rod, bar, and shapes; Ni-Cu alloy, plate, sheet, and strip; cartridge-brass cartridge case cups; com. bronze strip and bullet jacket cups; leaded high-strength yellow brass (Mn bronze) sand castings; Cu rod, bar, and shapes; brass wire; seamless brass tube; tests for sealing of, and of wt. of coating on, anodically coated Al; Mn bronze, phosphor bronze, and leaded red-brass rod, bar, and shapes; electrodeposited coatings of Ni and Cr on Cu and Cu-base alloys, and on Zn and Zn-base alloys; Sn-bronze, leaded Sn-bronze, and high-leaded Sn-bronze sand castings; leaded red-brass and leaded semi-red-brass sand castings; leaded yellow-brass, high-strength yellow-brass (Mn bronze), and leaded high-strength yellow-brass (leaded Mn bronze) sand castings; Al-bronze, leaded Ni-brass, and leaded Ni-bronze sand castings; Al-bronze rod, bar, and shapes; Cu-Ni-Zn alloy rod and bar; Cu sheet, strip, plate, and rolled bar; test for expansion of Cu and Cu-alloy tubing; HgNO3 test for Cu and Cu alloys; phosphor bronze wire; Ni rods, bars, seamless pipe and tubing, plate, sheet, and strip; seamless Ni and high-Ni alloy condenser, evaporator and heat-exchanged tubes; Ni-Cu alloy rods, bars, and seamless pipe and tubing; Ni-Cr-Fe alloy rods, bars, seamless pipe and tubing, plate, sheet, and strip; Al-bronze plate, sheet, strip, and rolled bar; O-free electrolytic Cu wire bars, billets, and cakes; Cu-alloy condenser-tube plates; rope-lay-stranded Cu conductors having bunch-stranded members and having concentric-stranded members for **elec**. **conductors**; bunchstranded Cu conductors; Cu-base alloy **die** castings; Cr plating on steel for engineering use; Al-alloy sheet and plate for pressure vessel; Al-base alloys in ingot form for sand castings, **die** castings, and permanent mold castings; test for effect of controlled atm. upon alloys in elec. furnaces; life test of elec. contact materials; prepn. of low-C and high-C steel for electroplating; Al and Al-alloy metal arc-welding electrodes; total, and alternate, immersion corrosion tests of nonferrous **metals**; **Cu** bus bar, rod, and shapes; seamless Cu bus pipe and tube; Pb-coated and Pb-alloy-**coated** soft **Cu** wire; Cr-Ni-Fe alloy castings (25-12 class); test for equiv. yield stress of thermostat **metals**; **Cu**-Be alloy plate, sheet, strip, rolled bar, rod, bar, and wire; Si-bronze and Si-brass sand castings; Mg-base alloy permanent mold castings; chromate finishes on electrodeposited Zn, hot-dipped galvanized, and Zn **die**-cast surfaces; metal powder sintered bearings; Cu-Ni-Zn alloy wire; Ni-Cr-Fe alloy castings (35-15 class) for high-temp. service; tension test specimens for Cu-base alloys for sand castings; Al-alloy sheet, plate, drawn seamless tubes, bar, rod,

and wire; tests for apparent d. and flow rate of metal powders; sieve and subsieve analysis of granular metal powders; sampling finished lots of metal powders; fire-refined Cu for wrought products and alloys; Mg-base-alloy extruded tubes; Al-alloy extruded bars, rods, and shapes; sintered metal powder structural parts; test for modulus of elasticity of thermostat **metals**; classification of **coppers**; Cu and Cu-alloy welding electrodes; cored, annular, concentric-lay-stranded Cu conductors; hard-drawn Cu-covered steel wire; concentric-lay-stranded Cu-covered steel conductors and Cu and Cu-covered steel composite conductors; hard-drawn Al wire for elec. purposes; concentric-lay-stranded Al conductors; rolled Al rods; Al-alloy drawn seamless tubes and extruded tubes; Al bars for elec. purposes; metallic Sb; Zn-base alloys in ingot form for **die** castings; Al-alloy pipe; definitions of terms used in powder metallurgy; measuring thickness of anodic coatings on Al; standard-wt. Zn-coated steel core wire for Al conductors; tinned hard-drawn and medium-hard-drawn Cu wire for elec. purposes; Al-alloy **die** forgings; requirements for wrought Cu and Cu-alloy plate, sheet, strip, rolled bar, bar, rod, shapes, and wire; requirements for wrought seamless Cu and Cu-alloy pipe and tube; prepn. of Zn-base **die** castings for electroplating; prepn. of and electroplating on Al alloys and stainless steel; sintered metal structural parts from bronze; standard nominal diams. and cross-sectional areas of AWG sizes of solid round wires used as **elec. conductors**; Cu and Cu-alloy welding rods; brazing filler metal; Zn-coated core wire for steel-reinforced Al conductors; 3/4 hard Al wire for elec. purposes; detn. of cross-sectional area of stranded conductors; Ti strip, sheet plate bar tube rod, and wire; high-resistivity, low-temp. coeff. wire; Cu-base alloy centrifugal castings; rectangular Cu wire; Al-alloy bars, rods, shapes, pipe, and tube for pressure-vessel applications; codification and temper designation of cast and wrought light metals and alloys; evaluating cemented carbides for apparent porosity; test for hardness of elec. contact materials; test for stiffness of bare soft square and rectangular Cu wire for magnet-wire fabrication; seamless Cu tube for refrigeration field service; prepn. of Cu and Cu-base alloys for electroplating; sintered metal powder structural parts from brass; Cu and Cu-alloy **die** forgings; rosin flux cored solder; Al and Al-alloy welding rods and bare electrodes; soft or annealed **coated Cu** conductors; HOAc-NaCl spray (fog) testing; Cu-Zn-Mn alloy (Mn brass) sheet and strip; hardness testing of cemented carbides; Ni and Ni-base-alloy covered welding electrodes; W arc-welding electrodes; Ag-coated soft or annealed Cu wire; Ti sponge; TeCu rod; threadless Cu pipe; Cu-infiltrated Fe parts; prepn, of micrographs of metals and alloys and of metallographic specimens; verification of testing machines; definitions of terms relating to metallography and to methods of mech. testing; methods of tension and compression testing of metallic materials; test for Brinell hardness, Rockwell hardness, and Rockwell superficial hardness of metallic materials; thermal analysis of metals and alloys; bend testing for ductility of metals; impact testing of metallic materials; definitions of terms relating to rheological properties of matter and to heat-treatment of metals; practices for designating significant places in specified limiting values; hardness conversion table for cartridge brass and for Ni and high-Ni alloys; identification of cryst. materials; industrial radiographic terminology for use in radiographic inspection of castings and weldments; sampling wrought nonferrous metals and alloys for detn. of chem. oomph.; verification of calibration devices for verifying testing machines; estg. av. grain size of wrought Cu and Cu-base alloys and other nonferrous metals, dilatometric analysis of metallic materials; prepg. quant. pole figures of metals; detg. orientation of a metal crystal; verification and classification of extensometers; test for diamond pyramid hardness of metallic materials; radiographic testing; radiographs for inspection of Al and Mg castings; rapid indentation hardness of metallic

materials; probability sampling of materials; detn. of Young's modulus at room temp.; detg. av. grain size of metals; ultrasonic testing by resonance and reflection methods; and round Cr-Cu wire for electronic devices. Cf. C.A. 47, 8613g.

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AN 1953:51133 HCAPLUS
DN 47:51133
OREF 47:8613g-i,8614a-i,8615a-e
TI American Society for Testing Materials, Standards, 1952. II. Nonferrous metals
SO (1952), 1327 pp.
DT Book
LA Unavailable
AB Standards or tentative standards, adopted or revised in 1952, are given for: hard-drawn, medium-hard-drawn, and soft or annealed Cu wire; tinned soft or annealed, Pb-coated and Pb-alloy-**coated Cu** wire for elec. purposes; soft rectangular, square bare Cu wire and hard-drawn Cu alloy wires for **elec. conductors**; hard-drawn Cu-covered steel wire; tinned hard-drawn and medium-hard-drawn Cu wire for elec. purposes; standard nominal diams. and cross-sectional areas of AWG sizes of solid round wires used as **elec. conductors**; bronze and Cu trolley wire; figure-9 deep-section grooved and figure-8 Cu trolley wire for industrial haulage; concentric-lay-stranded Cu conductors; rope-lay-stranded Cu conductors having bunch-stranded or concentric-stranded members for **elec. conductors**; bunch-stranded Cu conductors for **elec. conductors**; annular cored concentric-lay stranded Cu conductors; concentric-lay-stranded Cu-covered steel and Cu-covered steel composite conductors; hot-rolled Cu rods for elec. purposes; Cu bus bar, rod, and shapes; seamless Cu bus pipe and tube: test for resistivity of **elec. conductor** materials; hard-drawn and three-quarter hard-drawn Al wire for elec. purposes; hard-drawn and steel-reinforced concentric-lay-stranded Al conductors; Al bars and rolled Al rods for elec. purposes; classification of coppers; lake and electrolytic Cu wire bars, cakes, slabs, billets, ingots, and ingot bars; electrolytic cathode Cu; O-free electrolytic Cu wire, bars, billets, and cakes; fire-refined casting Cu, and Cu for wrought products and alloys; phosphor and S Cu; wrought Cu and Cu-alloy, brass and leaded brass plate, sheet, strip, and rolled bar; cartridge brass sheet, strip, plate, bar, disks, and cartridge-case cups; gilding metal strip and bullet-jacket cups; rolled Cu-alloy bearing and expansion plates and sheets; phosphor bronze, Cu-Ni-Zn-alloy, Cu-Ni-alloy, Al-bronze Cu-Si-alloy, and Cu-Be-alloy plate, sheet, strip, and rolled bar; Cu-Si-alloy plate and sheet for pressure vessels; Cu sheet, strip, plate, and rolled bar; Cu plates for locomotive fireboxes, Cu-alloy condenser tube plates; Pb-**coated Cu** sheets; hardness conversion table for cartridge brass; estg. av. grain size of wrought-Cu and Cu-base alloys; wrought-Cu and Cu-alloy rod, bar, and shapes; Cu rods for locomotive staybolts; free-cutting brass rod, bar, and shapes for use in screw machines; naval-brass, Cu-Si-alloy, Cu, Mn-bronze, phosphor-bronze, leaded-red-brass, and Al-bronze rod, bar, and shapes; Cu-Be-alloy rod and bar; Cu and Cu-base-alloy forging rod, bar, and shapes; Cu-Ni-Zn-alloy rod and bar; $HgNO_3$ test for Cu and Cu alloys; wrought-Cu and Cu-alloy wire; Cu-Si alloy and rectangular Cu wire for general purposes; brass, phosphor-bronze, Cu-Be-alloy, and Cu-Ni-Zn-alloy wire; wrought seamless Cu and Cu-alloy pipe and tube; Cu and Cu-alloy seamless condenser tubes and ferrule stock; seamless Cu boiler tube, Cu pipe, Cu tube, Cu water tube, brass boiler tube, red-brass pipe, and brass tube; test for expansion of Cu and Cu-alloy tubing; Cu-base alloys in ingot form for sand castings; cast Cu-base alloys; bronze castings for bridges and turntables; steam or valve bronze castings; compn. brass or

ounce metal castings; bronze castings for locomotive wearing parts; lined car and tender journal bearings; leaded high-strength yellow-brass, Sn-bronze, leaded Sn-bronze, high-leaded Sn-bronze, leaded red-brass, leaded semired-brass, leaded yellow-brass, high-strength yellow-brass, leaded high-strength yellow-brass, Al-bronze, leaded Ni-brass, leaded Ni-bronze, Si-bronze, and Si-brass sand castings; Cu-base alloy **die** and centrifugal castings; tension-test specimens for Cu-base alloys for sand castings; Cu and **Cu**-alloy **metal** arc-welding electrodes and welding rods; brazing filler metal; sampling wrought nonferrous metals and alloys for detn. of chem. compn.; Al for use in Fe or steel manuf.; Al ingots for remelting; Al-base alloys in ingot form for sand, **die**, and permanent mold castings; Al-base alloy sand, **die**, and permanent mold castings; Al-alloy **die** forgings; Al and Al-alloy bars, rods, wire, extruded bars, rods, and shapes; Al and Al-alloy bars, rods, and shapes for pressure vessels; Al and Al-alloy sheet, plate, pipe, and tube; Al-alloy pipe; Al-alloy drawn seamless and extruded tubes; Al-alloy drawn seamless tubes for condensers and heat exchangers; Al and Al-alloy metal arc-welding electrodes; dielec. strength of anodically coated Al; sealing of anodically coated Al; wt. of coating on anodically coated Al; measuring thickness of anodic coatings on Al; estg. av. grain size of nonferrous **metals**, other than **Cu**, and their alloys; prepn. of and electroplating on Al alloys; codification of cast and wrought light metals and alloys; Mg ingot and stick for remelting; Mg-base alloys in ingot form for sand, **die**, and permanent mold castings; Mg-base-alloy sand permanent mold and **die** castings; Mg-base-alloy sheet, forgings, bars, rods, and shapes; Mg-base-alloy extruded round tubes; slab and rolled Zn; Zn-base-alloy **die** castings; Zn-base alloys in ingot form for **die** castings; prepn. of Zn-base **die** castings for electroplating; metallic Sb; Pb- and Sn-base alloy **die** castings; pig lead; white-metal bearing alloys; soft solder metal; Ag solders; Ni; Ni, Ni-Cu-alloy, and Ni-Cr-Fe-alloy plate, sheet, and strip; 80% Ni, 20% Cr, and 60% Ni, 16% Cr, and balance Fe drawn or rolled alloy for elec.-heating element; Ni, Ni-Cu-alloy, and Ni-Cr-Fe-alloy rods and bars; round Ni wire for lamps and electronic devices; seamless Ni, Ni-Cu-alloy, and Ni-Cr-Fe-alloy pipe and tubing; Ni and high-Ni-alloy seamless condenser, evaporator, and heat-exchanger tubes; hardness conversion table for Ni and high-Ni alloys; Ti ingot; Ti strip, sheet, plate, bar, tube, rod, and wire; iodide Ti; test for change with temp. of metallic materials for elec. heating resistance; accelerated life test for metallic materials for elec. heating; high-resistivity, low-temp.-coeff. wire; test for resistivity of metallically conducting resistance and contact materials; test for thermoelec. power of **elec.-resistance** alloys; test for temp.-resistance consts. of alloy wires for precision resistors; test for temp.-resistance consts. of sheet materials for shunts and precision resistors; Cr-Ni-Fe- and Ni-Cr-Fe-alloy castings for high-temp. service; test for effect of controlled atms. upon alloys in elec. furnaces; circular cross-section Ni cathode sleeves for electronic devices; Cr-Cu wire for electronic devices; 17% and 28% Cr-Fe alloy for sealing to glass; bend testing of wire for radio tubes and incandescent lamps; testing sleeves and tubing for radio tube cathodes; test for temper of strip and sheet metals for electronic devices; testing wire for supports used in electronic devices and lamps; test for d. of fine wire and ribbon for electronic devices; test for strength of welded joints of lead wire for electronic devices and lamps; test for surface flaws in W seal rod and wire; test for diam. by weighing of fine wire used in electronic devices and lamps; measuring residual stress in cylindrical metal-to-glass seals; testing fine round and flat wire for electronic devices; test for sag of W wire; test for relative thermionic emissive properties of materials used in electron tubes; cathode melt prove-in testing; test for linear expansion of metals; life test of elec. contact

materials; testing thermostat metals; test for equiv. yield stress of thermostat metals; test for modulus of elasticity of thermostat metals; metal powder sintered bearings; sintered metal structural parts; test for apparent d., flow rate, and sieve analysis of metal powders; sampling finished lots of metal powders; evaluating microstructure of apparent porosity in cemented carbides; terms used in powder metallurgy; electrodeposited coatings of Zn, Cd, Pb, and Ni and Cr on steel; electrodeposited coatings of Ni and Cr on Cu and Cu-base and Zn and Zn-base alloys; chromate finishes on electrodeposited Zn, hot-dipped galvanized, and Zn **die**-cast surfaces; test for local thickness of electrodeposited coatings; salt-spray testing; Cr plating on steel for engineering use; prepn. of low- and high-C steels for electroplating; prepn. of and electroplating on stainless steel; alternate immersion corrosion tests and total immersion corrosion test of nonferrous metals; prepn. of micrographs of metals and alloys; prepn. of metallographic specimens; prepg. quant. pole figures of metals; detg. orientation of a metal crystal; x-ray diffraction of cryst. materials; and terms relating to metallography. Tentative revisions submitted in 1952 are given for: Cu and Cu-alloy seamless condenser tubes and ferrule stock; Mn-bronze rod, bar, and shapes; and method of accelerated life test for metallic materials for elec. heating.

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AN 1945:11851 HCAPLUS
DN 39:11851
OREF 39:1827a-i,1828a-i,1829a
TI American Society for Testing Materials, Standards, 1944. I. Metals
SO 2047 pp
DT Book
LA Unavailable
AB cf. C.A. 38, 3037.8. In addn. to standards previously published, standards adopted or revised in 1944 are given for: boiler and firebox steel for locomotives; plates of C steel, C-Si steel, chrome-Mn-Si alloy-steel, low-C Ni-steel, Mo-steel and Mn-V steel for boilers and other pressure vessels; boiler rivet steel and rivets; bars for springs of C-steel and of C-steel with special Si requirements; wrought-steel wheels; C-steel castings for miscellaneous industrial uses; C-steel and alloy-steel castings for railroads; alloy-steel castings for structural purposes; C-steel and alloy-steel castings for valves, flanges and fittings for high-temp. service; C-steel castings suitable for fusion welding for miscellaneous industrial uses; welded and seamless steel pipe and pipe piles; black and hot-dipped Zn-coated welded and seamless steel pipe for ordinary uses; **elec.-resistance**-welded steel pipe; spiral-welded steel or Fe pipe; welded alloyed open-hearth Fe pipe; lap-welded and seamless steel and lap-welded Fe boiler tubes; seamless low-C and C-Mo steel still tubes for refinery service; **elec. resistance**-welded steel and open-hearth Fe boiler tubes; seamless cold-drawn low-C steel and intermediate alloy-steel heat-exchanger and condenser tubes; seamless steel boiler tubes for high-pressure service; seamless intermediate alloy-steel still tubes for refinery service; seamless boiler and superheater tubes of alloy steel, C-Mo alloy steel and medium-C steel; **elec.-resistance**-welded steel heat-exchanger and condenser tubes; **elec.-resistance** -welded steel boiler and superheater tubes for high-pressure service; at.-H-arc-welded and **elec.-resistance**-welded alloy-steel boiler and superheater tubes; **elec.-resistance**-welded C-Mo alloy-steel boiler and superheater tubes; Cu-brazed steel tubing; forged or rolled alloy-steel pipe flanges, forged fittings and valves and parts for service at temps. from 750 to 1100.degree.F.; factory-made wrought C-steel and C-Mo-steel welded fittings; corrosion-resisting Cr-Ni and Cr-steel plate, sheet and strip;

alloy-steel castings for valves, flanges and fittings for service at temps. from 750 to 1100.degree.F.; forged or rolled alloy steel pipe flanges, forged fittings and valves and parts for service at temps. from 750 to 1100.degree.F.; at.-H-arc-welded and **elec.**-**resistance**-welded alloy-steel boiler and superheater tubes; seamless alloy-steel boiler and superheater tubes; welded and seamless black and hot-dipped Zn-coated steel pipe for ordinary uses; lap-welded and seamless steel and lap-welded Fe boiler tubes; tests for magnetic properties of Fe and steel; Al ingots for remelting; concentric-lay-stranded, hard, medium-hard or soft Cu conductors; rolled Cu-alloy bearing and expansion plates for bridge and other structural uses; Tentative standards issued or revised in 1944 are given for: structural quality, light gage, flat-rolled and flat hot-rolled C steel; C-steel and alloysteel blooms, billets and slabs for forgings; C-steel seamless drum forgings; magnetic particle testing and inspection of heavy steel forgings; C-steel and alloy-steel castings suitable for fusion welding; magnetic particle testing and inspection of com. steel castings; lab-welded and seamless steel pipe for high-temp. service; seamless alloy-steel and C-Mo alloy-steel pipe for service at temps. from 750 to 1100.degree.F.; seamless and welded ferritic and austenitic stainless steel tubing for general service; seamless and welded austenitic stainless steel tubing for the dairy and food industry; seamless austenitic Cr-Ni steel still tubes for refinery service; alloy-steel bolting materials for high-temp. service; heat-treated C-steel bolting material; corrosion-resisting Cr-Ni and Cr-steel clad plate, sheet and strip; Cr-Ni-Fe alloy castings for high-temp. service; hot-rolled and cold-finished corrosion-resisting steel bars; alloy-steel bolting materials for high-temp. service; seamless alloy-steel pipe for service at temps. from 750 to 1100.degree.F.; seamless austenitic Cr-Ni steel still tubes for refinery service; seamless and welded ferritic and austenitic stainless steel tubing for general service; seamless and welded austenitic stainless steel tubing for the dairy and food industry; boiling-HNO3 test for corrosion-resisting steels; hot-dip Pb coating on Fe or steel hardware; salt-spray testing; light-weight and thin-sectioned gray iron castings; automotive gray iron castings; gray iron castings for pressure-contg. parts for temps. up to 650.degree.F.; pearlitic malleable iron castings; malleable iron flanges, pipe fittings and valve parts; magnetic-particle testing and inspection of com. steel castings and of heavy steel forgings; definitions of terms, with symbols, relating to magnetic testing; prepn. of micrographs of metals and alloys including recommended practice for photography as applied to metallography; prepn. of metallographic specimens; ingot Al-base alloys for sand castings; Al-base alloy sand castings; Al-base alloys in ingot form for permanent mold castings; Al-base alloy permanent mold castings; ingot Al-base alloys for **die** castings; Al-base alloy **die** castings; Al-alloy bars, rods, wire and shapes; Al and Al-alloy sheet and plate; Al and Al-Mn alloy sheet and plate for use in welded pressure vessels; Al-Mn and Al-Mg-Cr alloy sheet and plate; alternate immersion corrosion test of nonferrous metals; Mg-base alloys in ingot form for sand castings and **die** castings; Mg-base alloy sand castings and **die** castings; Mg-base alloy bars, rods, shapes, forgings and sheets; O-free electrolytic Cu wire bars, billets and cokes; Pb-coated and Pb-alloy-**coated** soft **Cu** wire for elec. purposes; brass sheet and strip; leaded brass sheet and strip; cartridge-brass sheet, strip, plate, bar and disks; cartridge brass cartridge-case cups; gilding-metal strip; gildingmetal bullet-jacket cups; Al-bronze sheet and strip; Cu sheet, strip and plate; Cu-alloy condenser-tube plates; naval brass rods, bars and shapes; Cu bus bars, rods and shapes; Cu-base alloy forging rods, bars and shapes; Cu rods, bars and shapes; brass wire; phosphor-bronze rods, bars and shapes; Al bronze rods, bars and shapes; Cu-Ni-Zn alloy rod, bar and wire; phosphor-bronze wire; resistivity of Cu and Cu-alloy

elec. conductors; Cu bus pipes and tubes; Cu-base alloys in ingot form for sand castings; bronze castings for turntables and movable bridges and for bearing and expansion plates of fixed bridges; leaded high-strength yellow brass (Mn bronze) sand castings; Sn-bronze and leaded Sn-bronze sand castings; leaded red brass and leaded semi-red brass sand castings; leaded yellow brass sand castings for general purposes; high-strength yellow brass and high-strength leaded yellow brass sand castings; Al-bronze sand castings; leaded Ni-brass (leaded Ni-Ag) and leaded Ni-bronze (leaded Ni-Ag) sand castings; lead-coated and lead alloy-**coated** soft **Cu** wire for elec. purposes; Pb coating (hot-dip) on iron or steel hardware; drawn or rolled alloys (80% Ni, 20% Cr) (60% Ni, 16% Cr and rest Fe) for elec.-heating elements; test for equiv. yield stress of thermostat metals. Emergency standards issued or revised in 1944 are given for C-steel forgings for rings for main reduction gears; and for Al-base and Mg-base alloy special-quality **die** castings. For many of the standards emergency alternate provisions are included. Tentative revisions, submitted in 1944, of standards are given for steel for bridges and buildings; mild steel plates; low-tensile-strength C-steel plates of structural quality for welding; low-alloy structural steel; com.-quality hot-rolled bar steels, com. cold-finished bar steels and cold-finished shafting; C-steel and alloy-steel forgings for general industrial use and for locomotives and cars; C-steel and alloy-steel ring and disk forgings; elec.-fusion-welded steel pipe; wrought-Fe plates; automotive gray Fe castings; malleable Fe castings; cupola malleable Fe; methods of test for magnetic properties of Fe and steel; Mn-bronze rods, bars and shapes; leaded red brass rods, bars and shapes; and drawn or rolled alloys (80% Ni, 20% Cr) (60% Ni, 15% Cr, rest Fe) for elec.-heating elements.

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AN 1941:16335 HCAPLUS
DN 35:16335
OREF 35:2629f-i,2630f-i,2631a-b
TI American Society for Testing Materials, Standards, 1940 Supplement. I. Metals
SO 478 pp.
DT Book
LA Unavailable
AB cf. C. A. 34, 2957.9. Standards issued or revised in 1940 are given for structural-quality, low-tensile-strength C-steel plates for welding; boiler-rivet steel and rivets; com.-quality hot-rolled bar steels; castings for valves, flanges and fittings of C-steel for high-temp. service and of alloy steel for temps. of 750-1100.degree.F.; black and hot-dipped Zn-coated welded and seamless steel pipe for special and for ordinary uses; spiral-welded steel or iron pipe; lap-welded and seamless steel pipe for high-temp. service; lap-welded and seamless steel and lap-welded Fe boiler tubes; seamless steel boiler tubes for high-pressure service; seamless alloy-steel boiler and superheater tubes; **elec.-resistance**-welded steel and open-hearth-iron boiler tubes; **elec.-resistance**-welded steel boiler and superheater tubes for high-pressure service; seamless, medium-C steel boiler and superheater tubes; seamless cold-drawn low-C steel and alloy-steel heat-exchanger and condenser tubes; **elec.-resistance**-welded steel heat-exchanger and condenser tubes; seamless low-C and C-Mo steel and alloy-steel still tubes for refinery service; seamless intermediate alloy-steel still tubes for refinery service; pipe flanges, forged fittings and valves and parts of forged or rolled steel (for high-temp. service) or alloy steel (for 750-1100.degree.F.); C- and alloy-steel nuts for bolts for high-pressure and -temp. service; light-wt. and thin-sectioned gray iron castings; gray iron castings for valves, flanges and pipe fittings; automotive gray iron castings;

hard-drawn and medium-hard drawn Cu wire; Cu trolley wire for industrial haulage; steam or valve bronze castings; Cu-Si alloy rods, bars and shapes; seamless Cu boiler tubes; lead-**coated Cu** sheets; phosphor bronze sheet and strip; Cu-Si alloy sheet; Cu-Si alloy wire for general purposes; Cu-alloy, rolled, bearing and expansion plates for bridge and other structural uses; and method for testing thermostat metals. Tentative standards issued or revised in 1940 are given for Fe and steel arc-welding electrodes; heat-treated C- and alloy-steel track bolts and nuts; C- and alloy-steel forgings for general industrial use and for locomotives and cars; C-steel and alloy-steel castings suitable for fusion welding for service up to 850.degree.F. and 750-1100.degree.F., resp.; seamless alloy-steel and C-Mo alloy-steel pipe for service at 750-1100.degree.F. and 750-1000.degree.F., resp.; seamless C-Mo alloy-steel boiler and superheater tubes; factory-made wrought C-steel and C-Mo-steel welding fittings; alloy-steel bolting materials for high-temp. service; Cr-Ni corrosion-resisting steel sheet, strip and plate for fusion-welded unfired pressure vessels; test for uniformity of coating by the Preece test ($CuSO_4$ dip) on Zn-coated iron or steel articles; electrodeposited coatings of Cd on steel, Ni and Cr on steel and Zn on steel; test for local thickness of electrodeposited coatings on steel; test for measuring interlamination resistance and lamination factor of iron and steel; Al, Al-Mn-alloy and Al-Mg-Cr-alloy sheet and plate; Al-Mn alloy sheet and plate for use in welded pressure vessels; Al-alloy (duralumin) bars, rods, wire and shapes, and sheet and plate (Al-Cu-Mg-Mn); tests for sealing of, and for wt. of coating on, anodically coated Al; Mg-base alloys in ingot form for sand castings and **die** castings; Mg-base alloy sand castings, bars, rods, shapes, forgings and sheet; rectangular and square soft Cu wire for **elec.** **conductors**; Cu-base alloys in ingot form for sand castings; bronze castings for turntables and movable bridges and for bearing and expansion plates of fixed bridges; leaded high-strength yellow brass (Mn bronze) sand castings; classification of cast Cu-base alloys; Cu rods, bars and shapes; naval brass rods; brass pipe and tubes; Cu tubes; Cu and Cu-alloy seamless condenser tubes and ferrule stock; brass sheet, strip and wire; Be-Cu alloy bars, rods, sheet, strip and wire; Cu-Si alloy plate and sheet; cartridge-brass sheet, strip, disks and cartridge-case cups; gilding metal sheet and strip; gilding metal bullet jacket cups; pig lead; soft solder metal; Mg-base alloy **die** castings; testing of sleeves and tubing for radio-tube cathodes; and tension testing of metallic materials.

L68 ANSWER 1 OF 46 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:978551 HCAPLUS
DN 138:47095
TI Interconnect structure and process for silicon optical bench
IN Ray, Sudipta K.; Cohen, Mitchell S.; Herron, Lester Wynn; Interrante, Mario J.; Lombardi, Thomas E.; Shinde, Subhash L.
PA International Business Machines Corporation, USA
SO U.S. Pat. Appl. Publ., 10 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002196996	A1	20021226	US 2001-885791	20010620
PRAI	US 2001-885791		20010620		

AB A method of fabricating an optical subassembly in an **integrated circuit** is described entailing defining **elec. conducting** lines and bonding pads in a **metalization layer** (Cr/**Cu**/Ni/Au/Cr layers) on a substrate; depositing a passivation layer over the metalization layer; etching the passivation layer to remove the passivation layer from each of the bonding pads and a portion of the metalization layer assocd. with each of the bonding pads; diffusing Cr from the lines proximate the bonding pads to prevent solder wetting down lines; bonding an optical device to one of the bonding pads; and attaching the substrate to a carrier utilizing solder bond attachment. An optical subassembly in an **integrated circuit** is also described comprising a carrier having a first side and a second side; a ball grid array depending from the second side; a cavity disposed in the first side, a silicon optical bench (SiOB) having an optical device mounted thereon, the SiOB is elec. and mech. connected to the first side utilizing surface mount technol. attachment, the cavity providing clearance for the optical device when connecting the SiOB to the carrier, the SiOB having a metalization layer providing both wire bondable and solder bondable pads.

IT Electronic device fabrication
(interconnect structure and process for silicon optical bench)

IT Optical **integrated circuits**
(packages; interconnect structure and process for silicon optical bench)

IT **Polyimides**, uses
RL: DEV (Device component use); USES (Uses)
(passivation layer; interconnect structure and process for silicon optical bench)

IT 1333-74-0, Hydrogen, processes
RL: CPS (Chemical process); PEP (Physical, engineering or chemical process); PROC (Process)
(fluxless process; interconnect structure and process for silicon optical bench)

IT 7440-02-0, Nickel, uses 7440-47-3, Chromium, uses 7440-50-8, **Copper**, uses 7440-57-5, Gold, uses
RL: DEV (Device component use); USES (Uses)
(**metal layer**; interconnect structure and process for silicon optical bench)

IT 7440-21-3, Silicon, processes
RL: CPS (Chemical process); PEP (Physical, engineering or chemical process); PROC (Process)
(optical bench; interconnect structure and process for silicon optical bench)

IT 7631-86-9, Silica, uses 12033-89-5, Silicon nitride (Si3N4), uses

RL: DEV (Device component use); USES (Uses)
(passivation layer; interconnect structure and process for silicon optical bench)

IT 7440-31-5, Tin, processes 39460-91-8
RL: CPS (Chemical process); PEP (Physical, engineering or chemical process); PROC (Process)
(soldering; interconnect structure and process for silicon optical bench)

L68 ANSWER 2 OF 46 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:965067 HCAPLUS
DN 138:48323
TI Method for manufacturing semiconductor devices having copper interconnects imbedded in a low-k dielectric layer
IN Ting, Shao-yu; Liang, Jack; Liu, Kuo-ju
PA Taiwan
SO U.S. Pat. Appl. Publ., 10 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2002192937	A1	20021219	US 2002-42995	20020107
PRAI US 2001-294875P	P	20010530		

AB The invention relates to a dual damascene process for forming semiconductor devices contg. a copper interconnect and a low-k dielec. layer on a **wafer**, where the low-k dielec. layer is not degraded by a subsequent plasma etching. The process includes the steps of (i) forming a silica glass layer on a **wafer** surface which contains an interlevel dielec. (IDL) layer; (ii) photolithog. patterning the silica glass layer according to the pattern intended for the copper interconnect; (iii) conformably depositing a spacer dielec. layer on the silica glass layer; (iv) anisotropically etching the spacer dielec. layer to form a sidewall spacer; (v) depositing a low-k dielec. material on the **wafer** to form a low-k dielec. layer covering the silica glass layer and the sidewall spacer, followed by planarizing the low-k dielec. layer by chem.-mech. polishing; (vi) photolithog. removing the silica glass layer to form a trench in the low-k dielec. layer; (vii) depositing a **copper layer** to fill the trench; and (viii) planarizing the **copper layer**.

IT Etching
(anisotropic; method for manufg. semiconductor devices having copper interconnects imbedded in a low-k dielec. layer)

IT Polishing
(chem.-mech.; method for manufg. semiconductor devices having copper interconnects imbedded in a low-k dielec. layer)

IT Films
(**elec. conductive**; method for manufg. semiconductor devices having copper interconnects imbedded in a low-k dielec. layer)

IT Electric conductors
(films; method for manufg. semiconductor devices having copper interconnects imbedded in a low-k dielec. layer)

IT Polysiloxanes, uses
RL: DEV (Device component use); USES (Uses)
(fluoro, low-k dielec.; method for manufg. semiconductor devices having copper interconnects imbedded in a low-k dielec. layer)

IT **Polyimides**, uses
Polymers, uses
Silsesquioxanes
RL: DEV (Device component use); USES (Uses)

(low-k dielec.; method for manufg. semiconductor devices having copper interconnects imbedded in a low-k dielec. layer)
IT Dielectric films
(low-k, spacer; method for manufg. semiconductor devices having copper interconnects imbedded in a low-k dielec. layer)
IT Diffusion barrier
Electric contacts
Interconnections, electric
Photolithography
Semiconductor device fabrication
(method for manufg. semiconductor devices having copper interconnects imbedded in a low-k dielec. layer)
IT Electric insulators
(trench isolation; method for manufg. semiconductor devices having copper interconnects imbedded in a low-k dielec. layer)
IT 62974-64-5, Cobalt tungsten phosphide (CoWP)
RL: DEV (Device component use); USES (Uses)
(barrier; method for manufg. semiconductor devices having copper interconnects imbedded in a low-k dielec. layer)
IT 7440-06-4, Platinum, uses 7440-22-4, Silver, uses 7440-50-8, **Copper**, uses 7440-57-5, Gold, uses
RL: DEV (Device component use); USES (Uses)
(**metalization**; method for manufg. semiconductor devices having copper interconnects imbedded in a low-k dielec. layer)
IT 12033-89-5, Silicon nitride, uses 60676-86-0
RL: DEV (Device component use); USES (Uses)
(method for manufg. semiconductor devices having copper interconnects imbedded in a low-k dielec. layer)
IT 7631-86-9, Silica, uses
RL: DEV (Device component use); USES (Uses)
(modified, dielec.; method for manufg. semiconductor devices having copper interconnects imbedded in a low-k dielec. layer)

L68 ANSWER 3 OF 46 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:946663 HCAPLUS
DN 138:10640
TI Process for wiring electrical contact sites on the surface of a **microelectronic** component
IN Lowack, Klaus; Schmid, Guenter; Sezi, Recai; Zschieschang, Ute
PA Infineon Technologies AG, Germany
SO U.S. Pat. Appl. Publ., 6 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2002184756	A1	20021212	US 2002-145393	20020514
DE 2001-10126734	A	20010531		

PRAI
AB The invention relates to a process for wiring elec. contact sites on the surface of a **microelectronic** component to create thicker interconnects that can carry a greater c.d. The process involves the following steps: (i) applying and patterning at least one dielec. on the component surface; (ii) currentlessly depositing a conductor starting layer for producing metal wiring interconnects and substitute contact sites with short-circuit contacts for interconnecting the individual metal wiring interconnects and the corresponding elec. contact sites; (iii) reinforcing the conductor starting layer by a common electrodepositing process; and (iv) sepg. the short-circuit contacts for sepg. the elec. contact sites or the contact sites of the wiring from one another.
IT Polybenzimidazoles

Polybenzoxazoles
Polyimides, uses
Polysiloxanes, uses
RL: DEV (Device component use); USES (Uses)
(dielec.; process for wiring elec. contact sites on the surface of a **microelectronic** component)

IT Films
(**elec. conductive**; process for wiring elec. contact sites on the surface of a **microelectronic** component)

IT Coating process
(electroless; process for wiring elec. contact sites on the surface of a **microelectronic** component)

IT Electric conductors
(films; process for wiring elec. contact sites on the surface of a **microelectronic** component)

IT Electric fuses
(ground plane, electro, laser; process for wiring elec. contact sites on the surface of a **microelectronic** component)

IT Electric insulators
(isolation; process for wiring elec. contact sites on the surface of a **microelectronic** component)

IT Coating materials
(masking, non-metalizable; process for wiring elec. contact sites on the surface of a **microelectronic** component)

IT Electric contacts
Electrodeposition
Interconnections, electric
Microelectronic devices
Short circuits
(process for wiring elec. contact sites on the surface of a **microelectronic** component)

IT 7440-02-0, Nickel, uses 7440-50-8, **Copper**, uses
RL: DEV (Device component use); USES (Uses)
(conductive **layer**; process for wiring elec. contact sites on the surface of a **microelectronic** component)

IT 9003-56-9
RL: DEV (Device component use); USES (Uses)
(dielec.; process for wiring elec. contact sites on the surface of a **microelectronic** component)

L68 ANSWER 4 OF 46 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:869231 HCAPLUS
DN 137:361618
TI Metalized dielectric substrates for electronic article surveillance tags
IN Burke, Thomas F.
PA Micrometal Technologies Inc., USA
SO PCT Int. Appl., 27 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 2002091322	A2	20021114	WO 2002-US13893	20020502

W: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZM, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM
RW: GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW, AT, BE, CH,

CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR,
BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG

PRAI US 2001-288941P P 20010504
US 2001-309651P P 20010802

AB An electronic surveillance tag which is of small size and easy to deactivate with high reliability uses a metalized substrate. A thin metalized inorg./**polymeric** dielec. substrate is clad on both sides with metal, for fabrication into a resonant circuit tag. The dielec. layer contains a via hole there through, and is formed directly on a 1st conductive foil layer. A 2nd conductive metal layer is deposited on the dielec. layer and in the via hole to interconnect the two conductive layers. This construction is subsequently etched into an inductor and capacitor plates of the circuit using an etch resist. The circuit's deactivation reliability is enhanced by the uniformity/consistency of the substrate's crit. breakdown thickness by non-mech. means. It also eliminates the need to devote tag surface area for a mech. interconnect, and permits a smaller capacitor plate to maximize the available surface area for inductor coil turns, thereby enhancing the inductance and detection range of a given size tag or to produce smaller tags with the same detection range.

IT Films
(**elec. conductive**; metalized dielec. substrates for electronic article surveillance tags)

IT Electric conductors
(films; metalized dielec. substrates for electronic article surveillance tags)

IT Alarm devices
Anodization
Capacitor electrodes
Conducting polymers
Contact holes
Dielectric films
Electric coils
Etching
Foils
Sputtering
(metalized dielec. substrates for electronic article surveillance tags)

IT Metals, uses
Polymers, uses
RL: DEV (Device component use); USES (Uses)
(metalized dielec. substrates for electronic article surveillance tags)

IT Fluoropolymers, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PYP (Physical process); PROC (Process); USES (Uses)
(metalized dielec. substrates for electronic article surveillance tags)

IT **Integrated circuits**
(resonant; metalized dielec. substrates for electronic article surveillance tags)

IT 1344-28-1, Alumina, processes 7429-90-5, Aluminum, processes 7440-50-8, **Copper**, processes 9002-88-4, Polyethylene 9003-07-0, Polypropylene 9003-53-6, Polystyrene 11099-19-7
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PYP (Physical process); PROC (Process); USES (Uses)
(**metalized** dielec. substrates for electronic article surveillance tags)

L68 ANSWER 5 OF 46 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:770172 HCAPLUS
DN 137:287526
TI Barrier pads for **wafer-chip** packages with solder bump contacts for **integrated circuits**

IN Kelkar, Nikhil Vishwanath; Gee, Stephen A.
PA National Semiconductor Corporation, USA
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6462426	B1	20021008	US 2000-738122	20001214

PRAI US 2000-738122 20001214

AB An **integrated-circuit** device includes a semiconductor **die** having **elec. conductive** pads equipped with top passivation layer having multiple openings. The barrier base pads are placed in elec. contact with the conductive pads, cover the passivation layer openings, and prevent cracks from propagating through the **integrated circuit** device. The **integrated circuit chip** is attached to an external substrate by connecting the contact bumps to the bonding pads on electronic substrate.

IT **Integrated circuits**
(assembly of; barrier pads for **wafer-chip** packages with solder bumps for elec. **integrated circuits**)

IT Solders
(bumps; barrier pads for **wafer-chip** packages with solder bumps for elec. **integrated circuits**)

IT **Polyimides**, uses
RL: TEM (Technical or engineered material use); USES (Uses)
(pads with, for elec. circuit **chips**; barrier pads for **wafer-chip** packages with solder bumps for elec. **integrated circuits**)

IT Electric contacts
(semiconductor **chips** with; barrier pads for **wafer-chip** packages with solder bumps for elec. **integrated circuits**)

IT 7429-90-5, Aluminum, uses 7440-50-8, **Copper**, uses 12641-72-4
RL: MOA (Modifier or additive use); USES (Uses)
(**pads** with, for elec. circuit **chips**; barrier pads for **wafer-chip** packages with solder bumps for elec. **integrated circuits**)

IT **124221-30-3**
RL: TEM (Technical or engineered material use); USES (Uses)
(pads with, for elec. circuit **chips**; barrier pads for **wafer-chip** packages with solder bumps for elec. **integrated circuits**)

RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L68 ANSWER 6 OF 46 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:353947 HCAPLUS
DN 136:362633
TI Production process for semiconductor device
IN Mashino, Naohiro
PA Japan
SO U.S. Pat. Appl. Publ., 17 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2002053730	A1	20020509	US 2001-3448	20011023

PRAI JP 2000-323949 A 20001024

AB In the prodn. of semiconductor devices, a surface of the portion corresponding to the **chip** packaging area of the glass substrate is treated with plasma in a vacuum, a Si **chip** is bonded through its surface opposed to an electrode-bearing surface of the same to the activated surface of the glass substrate, and a wiring pattern having a predetd. configuration is formed in such a manner that a conductor exposed from the glass substrate is connected with an electrode of the Si **chip**.

IT Vapor deposition process
(chem., protective insulating layer; prodn. process for semiconductor device)

IT Electrodeposition
(copper; prodn. process for semiconductor device)

IT Films
(**elec. conductive**; prodn. process for semiconductor device)

IT Electric conductors
(films; prodn. process for semiconductor device)

IT Computers
(microprocessors; prodn. process for semiconductor device)

IT Etching
(plasma, dielec. layers; prodn. process for semiconductor device)

IT Capacitors
Dielectric films
Glass substrates
Interconnections, electric
Memory devices
Resistors
(prodn. process for semiconductor device)

IT High-silica glasses
RL: DEV (Device component use); USES (Uses)
(prodn. process for semiconductor device)

IT Epoxy resins, uses
Phosphosilicate glasses
Polyimides, uses
RL: DEV (Device component use); USES (Uses)
(protective insulating layer; prodn. process for semiconductor device)

IT 7429-90-5, Aluminum, uses 7440-25-7, Tantalum, uses 7440-32-6, Titanium, uses 7440-33-7, Tungsten, uses 7440-47-3, Chromium, uses
RL: DEV (Device component use); USES (Uses)
(conductor layer; prodn. process for semiconductor device)

IT 11110-87-5
RL: DEV (Device component use); USES (Uses)
(eutectic alloy solder; prodn. process for semiconductor device)

IT 11144-61-9
RL: DEV (Device component use); USES (Uses)
(lead-free solder; prodn. process for semiconductor device)

IT 7440-02-0, Nickel, uses 7440-22-4, Silver, uses 7440-50-8, **Copper**, uses 7440-57-5, Gold, uses
RL: DEV (Device component use); USES (Uses)
(**metal** bump; prodn. process for semiconductor device)

IT 14808-60-7, Quartz, uses
RL: DEV (Device component use); USES (Uses)
(prodn. process for semiconductor device)

IT 1303-00-0, Gallium arsenide, uses 7440-21-3, Silicon, uses
RL: DEV (Device component use); USES (Uses)
(semiconductor **chip**; prodn. process for semiconductor device)

IT 7631-86-9, Silica, uses
RL: DEV (Device component use); USES (Uses)
(substrate; prodn. process for semiconductor device)

L68 ANSWER 7 OF 46 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:290838 HCAPLUS
DN 136:318003
TI Methods of fabricating a metal-oxide-metal capacitor with conducting layer encapsulated by tow dielectric layers and associated apparatuses in MOS devices
IN Harris, Edward Belden; Yan, Yifeng Winston; Merchant, Sailesh Mansinh
PA Agere Systems Guardian Corp., USA
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6373087	B1	20020416	US 2000-652479	20000831
	GB 2371675	A1	20020731	GB 2001-21040	20010830
	JP 2002237523	A2	20020823	JP 2001-262994	20010831
PRAI	US 2000-652479	A	20000831		

AB A method of fabricating a metal-oxide-metal capacitor in a **microelectronic** device is provided. First, a recess is formed in a surface of a dielec. layer deposited over a **microelectronic** substrate. A 1st barrier layer is then deposited over the dielec. layer such that the 1st barrier layer conforms to the recess. A 1st conductive element is then deposited over the 1st barrier layer so as to at least fill the recess. A 2nd barrier layer is further deposited over the 1st conductive element such that the 1st barrier layer and the 2nd barrier layer cooperate to encapsulate the 1st conductive element. The 1st conductive element thus comprises a 1st plate of the capacitor. A capacitor dielec. layer is then deposited over the 2nd barrier layer, followed by the deposition of a 2nd conductive element over the capacitor dielec. layer. The 2nd conductive element thus comprises a 2nd plate of the capacitor. In 1 embodiment, the dielec. layer may be comprised of an oxide and the barrier layers are comprised of, e.g., Ta; Ta nitride; Ti nitride; W nitride; Si nitrides of Ta, Ti, and W; and combinations thereof. The 1st conductive element is preferably comprised of Cu. The capacitor dielec. may be comprised of an oxide or Ta pentoxide, while the 2nd conductive element may be comprised of a layer of an Al alloy disposed between 2 barrier layers, each comprised of, e.g., Ta; Ta nitride; Ti nitride; W nitride; Si nitrides of Ta, Ti, and W; and combinations thereof. Assocd. apparatuses are also provided.

IT Polishing
(chem.-mech.; methods of fabricating a metal-oxide-metal capacitor and assocd. apparatuses)
IT **Polyimides**, uses
RL: DEV (Device component use); USES (Uses)
(dielec. layer; methods of fabricating a metal-oxide-metal capacitor and assocd. apparatuses)
IT Films
(**elec. conductive**; methods of fabricating a metal-oxide-metal capacitor and assocd. apparatuses)
IT Electric conductors
(films; methods of fabricating a metal-oxide-metal capacitor and assocd. apparatuses)
IT Capacitors
Dielectric films
Diffusion barrier
Electrodeposition
Encapsulation
Microelectronic devices

(methods of fabricating a metal-oxide-metal capacitor and assocd. apparatuses)
IT Aluminum alloy, base
RL: DEV (Device component use); USES (Uses)
(conducting layer; methods of fabricating a metal-oxide-metal capacitor and assocd. apparatuses)
IT 7440-25-7, Tantalum, uses 12033-62-4, Tantalum nitride 25583-20-4, Titanium nitride (TiN) 37359-53-8, Tungsten nitride 99039-55-1, Tantalum nitride silicide
RL: DEV (Device component use); USES (Uses)
(barrier layer; methods of fabricating a metal-oxide-metal capacitor and assocd. apparatuses)
IT 7429-90-5, Aluminum, uses 7440-05-3, Palladium, uses 7440-06-4, Platinum, uses 7440-22-4, Silver, uses 7440-32-6, Titanium, uses 7440-50-8, **Copper**, uses 7440-57-5, Gold, uses
RL: DEV (Device component use); USES (Uses)
(conducting **layer**; methods of fabricating a metal-oxide-metal capacitor and assocd. apparatuses)
IT 108729-83-5, Tungsten nitride silicide 121368-53-4, Titanium nitride silicide
RL: DEV (Device component use); USES (Uses)
(methods of fabricating a metal-oxide-metal capacitor and assocd. apparatuses)
IT 7440-21-3, Silicon, uses
RL: DEV (Device component use); USES (Uses)
(substrate; methods of fabricating a metal-oxide-metal capacitor and assocd. apparatuses)
RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L68 ANSWER 8 OF 46 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:204856 HCAPLUS
DN 136:248699
TI Primarily and secondary processed products of **polyimide**-coated substrates
IN Oguchi, Takahisa; Yamashita, Wataru
PA Mitsui Chemicals Inc., Japan
SO Jpn. Kokai Tokkyo Koho, 10 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2002079634	A2	20020319	JP 2000-269611	20000906
PRAI	JP 2000-269611		20000906		

AB The primarily processed products are obtained by punching, cutting, piercing, etching, polishing, plating, bending, or squeezing substrates coated with **polyimides** manufd. from 2,5(6)-di(aminomethyl)norbornene and tetarcarboxylic acid dianhydrides. The secondarily processed products are obtained by bonding the primarily processed products with other materials. Thus, GT-MP (electrolytic **Cu** foil) was **coated** with a varnish contg. 2,5(6)-diaminomethylbicyclo[2.2.1]-heptane-4,4'-(p-phenylenedioxy)diphthalic dianhydride copolymer, dried, etched, pierced, plated, cut, bent, squeezed, polished, and bonded with a glass substrate for liq. crystal display.
IT Acrylic polymers, uses
RL: TEM (Technical or engineered material use); USES (Uses)
(adhesives; secondary processed products of **polyimide**-coated substrates bonded via)

RL: TEM (Technical or engineered material use); USES (Uses)
(substrates, GT-MP; **polyimide**-coated substrates with good processability)

L68 ANSWER 9 OF 46 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:167687 HCAPLUS
DN 136:225230
TI Procedure for the fabrication of substrates for ball grid arrays
IN Le, Xie Wan; Cheng, Chuang Yung; Ning, Huang; Pin, Chen Hui; Wen, Chiang Hua; Ming, Chang Chuang; Chang, Tu Feng; Yu, Huang Fu; Jui, Chang Hsuan; Chieh, Hu Chia
PA Orient Semiconductor Electronics Ltd., Taiwan
SO Ger. Offen., 10 pp.
CODEN: GWXXBX
DT Patent
LA German
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI DE 10041872	A1	20020307	DE 2000-10041872	20000825
PRAI DE 2000-10041872		20000825		

AB The present invention provides a procedure for producing substrates for use in ball grid arrays. The procedure for the prodn. of the substrates comprises the following steps: forming a **polyimide** film as a carrier, electroplating a thin **Cu layer** and a thick **Cu layer** on the **polyimide** film, applying light-sensitive protective layers on both sides of the carrier, attaching 2 masks with optically transparent conducting paths on it, exposing and developing the carrier for removing the light-sensitive protective layers and for forming conducting lines on it, electroplating a further **Cu layer** on the top side of the carrier such that its top side is under that of the 1st light-sensitive protective layer, etching the lower surface of the carrier for removing the conductive line, **coating** the **Cu layer** with a solder material so that the **coated Cu layer** is even with the light-sensitive protective layer, cleaning the light-sensitive protective layers, and removing the excess **Cu layer**.

IT Semiconductor devices
(ball grid array; procedure for fabrication of substrates for ball grid arrays)
IT **Polyimides**, uses
RL: DEV (Device component use); USES (Uses)
(**chip** carrier; procedure for fabrication of substrates for ball grid arrays)
IT Films
(**elec. conductive**; procedure for fabrication of substrates for ball grid arrays)
IT Electric conductors
(films; procedure for fabrication of substrates for ball grid arrays)
IT Electrodeposition
Etching
Metal lines
Photomasks (lithographic masks)
Semiconductor device fabrication
(procedure for fabrication of substrates for ball grid arrays)
IT 7440-50-8, Copper, uses
RL: DEV (Device component use); USES (Uses)
(procedure for fabrication of substrates for ball grid arrays)

L68 ANSWER 10 OF 46 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:155205 HCAPLUS

DN 136:209096
TI Semiconductor devices containing **IC chips** mounted on UFPLs (ultra fine pitch lead-frame) and their manufacture
IN Makino, Haruhiko; Iwashita, Akira
PA Sony Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 12 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 2002064174	A2	20020228	JP 2000-250239	20000821
PRAI JP 2000-250239		20000821		

AB Semiconductor devices contain: inner leads for forming interconnection patterns, resin layers (e.g., **polyimides**) covering the top and bottom surfaces of the inner leads, partially exposed outer leads (e.g., **Cu**), **die pads** connected, in single units, to exposed heat-dispersing terminals, **IC chips** mounted on the **die** pads, interconnection wires connecting the **chip** electrodes and the inner lead surface, and packages sealing the **chips**, **die** pads, the inner leads, resin layers, wires, and parts of the outer leads. In the device manuf., the outer leads, **die** pads, and the terminals are formed by selectively etching metal plates. The **IC chips** may be adhered to the **die** pads using highly thermally conductive pastes. The semiconductor devices have excellent heat dispersion characteristic.

IT Heat
Integrated circuits
(heat dispersion of semiconductor devices contg. **IC chips** mounted on lead frames)
IT Thermal conductors
(heat dispersion of semiconductor devices contg. **IC chips** mounted on lead frames using thermally-**conductive elec.-conductive** pastes)
IT **Polyimides**, uses
RL: DEV (Device component use); USES (Uses)
(manuf. of semiconductor devices contg. **IC chips** and inner leads covered with resin layers)
IT Electronic packaging process
(manuf. of semiconductor devices contg. **IC chips** mounted on lead frames)
IT Etching
(of metal plates in manuf. of semiconductor devices contg. **IC chips** mounted on lead frames)
IT **Electrically conductive** pastes
(thermally-conductive; heat dispersion of semiconductor devices contg. **IC chips** mounted on lead frames using)
IT 7440-50-8, Copper, uses
RL: DEV (Device component use); USES (Uses)
(outer leads; semiconductor devices contg. **IC chips** mounted on UFPLs (ultra fine pitch lead-frame) and their manuf.)

L68 ANSWER 11 OF 46 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:51876 HCAPLUS
DN 136:111228
TI manufacturing electronic device with coil, capacitor and capacitor electrode
IN Pulsford, Nicolas Jonathan; Van Beek, Jozef Thomas Martinus
PA Neth.
SO U.S. Pat. Appl. Publ., 5 pp.

CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002006024	A1	20020117	US 2001-782664	20010213
PRAI	EP 2000-200496	A	20000215		

AB The electronic device of the invention has a 1st inductor and a 1st capacitor. The capacitor comprises a 1st capacitor electrode in a 1st **elec. conducting** layer, a dielec., and a 2nd capacitor electrode in a 2nd **elec. conducting** layer. The 2nd conductive layer also comprises the 1st inductor and a via. In order to get a resonance frequency with a low tolerance, which can be used at high frequencies in RF equipment, the 2nd capacitor electrode has a contour whose projection onto the 1st conductive layer lies within the 1st capacitor electrode. In this way the decrease in capacitance of the 1st capacitor due to etching can be leveled out against the increase in inductance of the 1st inductor due to the same etching. Preferably, the dielec. has a middle zone and edge zones. The dielec. consists of a layer of dielec. material in the middle zone. In the edge zones, the dielec. consists of the layer of dielec. material and a layer of elec. insulating material.

IT Polyanilines
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(conducting layer; electronic device with coil, capacitor and capacitor electrode)

IT **Polyimides**, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(dielec. film; electronic device with coil, capacitor and capacitor electrode)

IT Films
(**elec. conductive**; electronic device with coil, capacitor and capacitor electrode)

IT Capacitor electrodes
Capacitors
Dielectric films
Electric contacts
Etching
Microelectronic devices
Photolithography
(electronic device with coil, capacitor and capacitor electrode)

IT Electric conductors
(films; electronic device with coil, capacitor and capacitor electrode)

IT Electric coils
(inductor; electronic device with coil, capacitor and capacitor electrode)

IT Glass, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(substrate; electronic device with coil, capacitor and capacitor electrode)

IT Interconnections, electric
(vias; electronic device with coil, capacitor and capacitor electrode)

IT 7429-90-5, Aluminum, processes 7440-02-0, Nickel, processes 7440-06-4, Platinum, processes 7440-50-8, **Copper**, processes 7440-57-5, Gold, processes 126213-51-2
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)

(conducting **layer**; electronic device with coil, capacitor and capacitor electrode)

IT 7631-86-9, Silicon oxide, processes 12033-89-5, Silicon nitride, processes 12047-27-7, Barium titanate, processes 12672-32-1, Barium niobate 59269-51-1, Polyvinylphenol 59763-75-6, Tantalum oxide **124221-30-3**
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(dielec. film; electronic device with coil, capacitor and capacitor electrode)

IT 7440-21-3, Silicon, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(doped, conducting layer; electronic device with coil, capacitor and capacitor electrode)

IT 1344-28-1, Alumina, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(substrate; electronic device with coil, capacitor and capacitor electrode)

L68 ANSWER 12 OF 46 HCAPLUS COPYRIGHT 2003 ACS
AN 2001:712848 HCAPLUS
DN 135:273890
TI Manufacture of sheets with anisotropically electric conductivity
IN Komemoto, Ryuji
PA Hitachi Cable, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001266670	A2	20010928	JP 2000-75926	20000317
PRAI	JP 2000-75926		20000317		

AB Title sheets are prepd. by electrostatically flocking short elec. insulated **film-coated Cu** wire flakes on elec. insulating varnish films (A, preferably with room temp. modulus of .ltoreq.103 MPa), hardening the film A, and making the flocked flakes into **elec. conductive** passages. Spreading nitrile rubber particle-contg. epoxy resin adhesive (with modulus 400-103 MPa) on a PET film, electrostatically flocking short **polyimide-coated Cu** wires on the adhesives, curing the adhesive at 90-150.degree., peeling the PET film, abrading the flocked sheet, and electroless plating Sn on the **coated Cu** wire edges gave a title sheet, which was used in assembling semiconductor **chips** and showed no improper contact after 500 times heat cycles.

IT **Polyimides**, uses
RL: TEM (Technical or engineered material use); USES (Uses)
(elec. insulating coatings; manuf. of anisotropically **elec. conductive** sheets by electrostatically flocking insulated **film-coated Cu** flakes on adhesives of low modulus)

IT Metals, uses
RL: TEM (Technical or engineered material use); USES (Uses)
(electroless plating; manuf. of anisotropically **elec. conductive** sheets by electrostatically flocking insulated **film-coated Cu** flakes on adhesives of low modulus)

IT Semiconductor devices

(manuf. of anisotropically **elec. conductive** sheets by electrostatically flocking insulated **film-coated Cu** flakes on adhesives of low modulus)

IT Epoxy resins, uses
RL: POF (Polymer in formulation); PRP (Properties); TEM (Technical or engineered material use); USES (Uses)
(manuf. of anisotropically **elec. conductive** sheets by electrostatically flocking insulated **film-coated Cu** flakes on adhesives of low modulus)

IT Nitrile rubber, uses
RL: MOA (Modifier or additive use); USES (Uses)
(particles, in adhesives; manuf. of anisotropically **elec. conductive** sheets by electrostatically flocking insulated **film-coated Cu** flakes on adhesives of low modulus)

IT Adhesives
Electric conductors
(sheets; manuf. of anisotropically **elec. conductive** sheets by electrostatically flocking insulated **film-coated Cu** flakes on adhesives of low modulus)

IT 7440-31-5, Tin, uses 7440-57-5, Gold, uses 11110-87-5
RL: TEM (Technical or engineered material use); USES (Uses)
(electroless plating; manuf. of anisotropically **elec. conductive** sheets by electrostatically flocking insulated **film-coated Cu** flakes on adhesives of low modulus)

IT 9003-18-3
RL: MOA (Modifier or additive use); USES (Uses)
(nitrile rubber, particles, in adhesives; manuf. of anisotropically **elec. conductive** sheets by electrostatically flocking insulated **film-coated Cu** flakes on adhesives of low modulus)

IT 7440-50-8, Copper, uses
RL: TEM (Technical or engineered material use); USES (Uses)
(wire, short insulated film-coated flakes; manuf. of anisotropically **elec. conductive** sheets by electrostatically flocking insulated **film-coated Cu** flakes on adhesives of low modulus)

L68 ANSWER 13 OF 46 HCAPLUS COPYRIGHT 2003 ACS
AN 2001:645676 HCAPLUS
DN 135:188730
TI Non-metallic diffusion barrier formation for copper damascene type interconnects to prevent fluorine outdiffusion from fluorinated dielectric films
IN Chooi, Simon; Gupta, Subhash; Zhou, Mei-Sheng; Hong, Sangki
PA Chartered Semiconductor Manufacturing Ltd., Singapore
SO U.S., 12 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6284657	B1	20010904	US 2000-512379	20000225
	SG 87919	A1	20020416	SG 2001-873	20010216
	US 2001049195	A1	20011206	US 2001-925819	20010810
	US 6531390	B2	20030311		
	US 2001055878	A1	20011227	US 2001-925822	20010810
	US 2002001951	A1	20020103	US 2001-925820	20010810
	US 6429122	B2	20020806		

US 2002001952 A1 20020103 US 2001-925821 20010810
US 6489233 B2 20021203
PRAI US 2000-512379 A 20000225

AB A method for forming dual-damascene type conducting interconnects with nonmetallic barriers that protect said interconnects from F out-diffusion from surrounding low-k, fluorinated dielec. materials. One embodiment of the method is particularly suited for forming such interconnects in **microelectronics** fabrications of the sub 0.15 .mu.m generation.

IT Vapor deposition process
(chem.; non-metallic diffusion barrier formation for copper damascene type interconnects to prevent fluorine outdiffusion from fluorinated dielec. films)

IT Films
(**elec. conductive**; non-metallic diffusion barrier formation for copper damascene type interconnects to prevent fluorine outdiffusion from fluorinated dielec. films)

IT Electric conductors
(films; non-metallic diffusion barrier formation for copper damascene type interconnects to prevent fluorine outdiffusion from fluorinated dielec. films)

IT **Polyimides**, processes
RL: PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(fluorinated; non-metallic diffusion barrier formation for copper damascene type interconnects to prevent fluorine outdiffusion from fluorinated dielec. films)

IT Hydrocarbons, processes
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(fluoro, plasma etchants; non-metallic diffusion barrier formation for copper damascene type interconnects to prevent fluorine outdiffusion from fluorinated dielec. films)

IT Fluoride glasses
Silicate glasses
RL: PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(fluorosilicate; non-metallic diffusion barrier formation for copper damascene type interconnects to prevent fluorine outdiffusion from fluorinated dielec. films)

IT Etching
Lithography
(in non-metallic diffusion barrier formation for copper damascene type interconnects to prevent fluorine outdiffusion from fluorinated dielec. films)

IT Dielectric films
Diffusion barrier
Interconnections (electric)
Passivation
(non-metallic diffusion barrier formation for copper damascene type interconnects to prevent fluorine outdiffusion from fluorinated dielec. films)

IT Fluoropolymers, processes
RL: PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(non-metallic diffusion barrier formation for copper damascene type interconnects to prevent fluorine outdiffusion from fluorinated dielec. films)

IT Vapor deposition process
(phys.; non-metallic diffusion barrier formation for copper damascene type interconnects to prevent fluorine outdiffusion from fluorinated dielec. films)

IT Etching
(plasma; non-metallic diffusion barrier formation for copper damascene type interconnects to prevent fluorine outdiffusion from fluorinated dielec. films)
IT Interconnections (electric)
(vias; non-metallic diffusion barrier formation for copper damascene type interconnects to prevent fluorine outdiffusion from fluorinated dielec. films)
IT 409-21-2, Silicon carbide (SiC), processes 10043-11-5, Boron nitride, processes 12069-32-8, Boron carbide 12656-55-2, Boron carbide nitride 154769-61-6, Carbon nitride
RL: PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(barrier; non-metallic diffusion barrier formation for copper damascene type interconnects to prevent fluorine outdiffusion from fluorinated dielec. films)
IT 7440-25-7, Tantalum, processes 7440-32-6, Titanium, processes 7440-33-7, Tungsten, processes 7440-50-8, **Copper**, processes 9002-84-0, Teflon 11099-19-7 12033-62-4, Tantalum nitride (TaN) 12033-89-5, Silicon nitride, processes 12058-38-7, Tungsten nitride (WN) 13463-67-7, Titanium dioxide, processes 25583-20-4, Titanium nitride TiN
RL: PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(non-**metallic** diffusion barrier formation for copper damascene type interconnects to prevent fluorine outdiffusion from fluorinated dielec. films)
IT 630-08-0, Carbon monoxide, uses 1333-74-0, Hydrogen, uses 7440-37-1, Argon, uses 7727-37-9, Nitrogen, uses 7782-44-7, Oxygen, uses 7782-50-5, Chlorine, uses 10035-10-6, Hydrogen bromide, uses
RL: NUU (Other use, unclassified); USES (Uses)
(plasma etchants; non-metallic diffusion barrier formation for copper damascene type interconnects to prevent fluorine outdiffusion from fluorinated dielec. films)
IT 2551-62-4, Sulfur hexafluoride
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(plasma etchants; non-metallic diffusion barrier formation for copper damascene type interconnects to prevent fluorine outdiffusion from fluorinated dielec. films)
RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L68 ANSWER 14 OF 46 HCAPLUS COPYRIGHT 2003 ACS
AN 2000:814774 HCAPLUS
DN 133:358177
TI Method for manufacturing a printed circuit board with integrated heat sink for semiconductor package
IN Juskey, Frank J.; McMillan, John R.; Huemoeller, Ronald P.
PA Amkor Technology, Inc., USA
SO PCT Int. Appl., 24 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 2000069239	A1	20001116	WO 2000-US13041	20000511
	W: CA, JP, KR, SG				
	RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
	US 6337228	B1	20020108	US 1999-310660	19990512

US 2002043402 A1 20020418 US 2001-6642 20011205
US 6507102 B2 20030114
PRAI US 1999-310660 A 19990512

AB A low-cost printed circuit board (10) for a semiconductor package having the footprint of a ball grid array package has an integral heat sink (20), or slug, for the mounting of one or more semiconductor **chips**, capable of efficiently conducting away at least five watts from the package in typical applications. It is made by forming an opening (16) through a sheet, or substrate (14), of B-stage epoxy/fiberglass composite, or pre-preg, then inserting a slug (20) of a thermally conductive material having the same size and shape as the opening into the opening. The slug-contg. composite is sandwiched between two thin layers (30) of a conductive **metal**, preferably **Cu**, and the resulting sandwich (10) is simultaneously pressed and heated between the platen (12) of a heated press. The heat and pressure forces the resin to the surface of the composite (10) and into the space between the slug (20) and the walls of the composite, where it solidifies, bonding the edges of the slug (20) to the substrate (14) within the opening and adhering the conductive layers (30) to the upper and lower surfaces of the substrate (14). The resulting laminate (10) can thereafter be processed as a convention printed circuit board to incorporate conventional circuit board features, e.g., circuit traces, wire bonding pads, solder ball mounting lands, and via holes.

IT **Polyimides**, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(bismaleimide-based, triazine group-contg.; manufg. printed circuit board with integrated heat sink for semiconductor package)

IT Films
Films
(**elec. conductive**; manufg. printed circuit board with integrated heat sink for semiconductor package)

IT Electric conductors
Electric conductors
(films; manufg. printed circuit board with integrated heat sink for semiconductor package)

IT Contact holes
Dielectric films
Electronic device fabrication
Electronic packages
Electronic packaging process
Heat sinks
Heat treatment
Joining
Lamination
Printed circuit boards
Thermal conductors
(manufg. printed circuit board with integrated heat sink for semiconductor package)

IT Epoxy resins, processes
Glass fibers, processes
Polyimides, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(manufg. printed circuit board with integrated heat sink for semiconductor package)

IT Molding
(press; manufg. printed circuit board with integrated heat sink for semiconductor package)

IT Plastics, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical

process); PROC (Process); USES (Uses)
(thermosetting; manufg. printed circuit board with integrated heat sink for semiconductor package)
IT 7440-50-8, Copper, processes 25068-38-6, Epichlorohydrin-bisphenol A copolymer
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(manufg. printed circuit board with integrated heat sink for semiconductor package)
RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L68 ANSWER 15 OF 46 HCAPLUS COPYRIGHT 2003 ACS
AN 2000:744539 HCAPLUS
DN 134:49704
TI Fully additive **copper metallization** on BCB
AU Stolle, Thomas; Schwencke, Beatrice; Reichl, Herbert
CS FhG-IZM Berlin, Berlin, 13355, Germany
SO EUROMAT 99, Biannual Meeting of the Federation of European Materials Societies (FEMS), Munich, Germany, Sept. 27-30, 1999 (2000), Meeting Date 1999, Volume 13, 96-101. Editor(s): Grassie, K. Publisher: Wiley-VCH Verlag GmbH, Weinheim, Germany.
CODEN: 69AMNI
DT Conference
LA English
AB A fully additive **copper metalization** process on **benzocyclobutene** Cyclotene (BCB) was studied for application in MCM-D technol. The process consists of surface pretreatment of the BCB basic layer by reactive ion etching (RIE), spin-coating and photopatterning of an org. seed layer by broad-band I-line photolithog. followed by developing and activation steps. The metalization of the seed patterns was performed by a 2-step process by electroless copper baths. A height of .apprx.5 .mu.m selectively deposited copper can be achieved. The **elec. cond.** of patterns is in the range of 80% - 85% of the bulk cond. of pure copper. Adhesive strength tests during accelerated aging show good adhesion of copper to the BCB surface, which is influenced by RIE pretreatment, exposure dose and thermal load. Shear expts. performed with optimal treated 200.times.200 .mu.m bumps show shear forces > 150 cN. Design rules have to take into account the lateral growth of copper patterns, which is nearly equal to the vertical growth. Real spaces of .gtoreq. 30 .mu.m between copper lines are possible. The process is considered as a low cost technol. because of replacing of sputter technique, few process steps and waste redn.
IT Sputtering
(etching, reactive; fully additive **copper metalization** on BCB)
IT Adhesion, physical
Electric conductivity
Semiconductor device fabrication
(fully additive **copper metalization** on BCB)
IT Coating process
(**metalization**; fully additive **copper metalization** on BCB)
IT **Integrated circuits**
Semiconductor devices
(multichip module; fully additive **copper metalization** on BCB)
IT Etching
(sputter, reactive; fully additive **copper metalization** on BCB)
IT 2758-06-7, BCB

RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PRP (Properties); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(fully additive **copper metalization** on BCB)

IT 7440-50-8, Copper, uses
RL: TEM (Technical or engineered material use); USES (Uses)
(fully additive **copper metalization** on BCB)

RE.CNT 11 THERE ARE 11 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L68 ANSWER 16 OF 46 HCAPLUS COPYRIGHT 2003 ACS
AN 2000:380457 HCAPLUS
DN 133:170810
TI Reaction dynamics of CW Ar+ laser induced copper direct writing from liquid electrolyte on **polyimide** substrates
AU Kordas, K.; Nanai, L.; Galbacs, G.; Uusimaki, A.; Leppavuori, S.; Bali, K.
CS Department of Experimental Physics, Jozsef Attila University, Szeged, H-6720, Hung.
SO Applied Surface Science (2000), 158(1-2), 127-133
CODEN: ASUSEE; ISSN: 0169-4332
PB Elsevier Science B.V.
DT Journal
LA English
AB Conductive Cu patterns were deposited on **polyimide** (PI) surfaces using a focused, scanned continuous-wave Ar+ laser beam at 488-nm wavelength. The deposition process was initiated by a photo-thermal reaction of a tartrate-complex soln. of Cu2+ ions in an alk. and reducing medium. Deposits were characterized by field emission scanning electron microscope (FESEM), energy dispersive x-ray spectrometry (EDS) and resistance measurements. The mass of the deposited Cu (mCu) and also the rate of the deposition (dmCu/dt) were calcd. from the resistance measurements. The dependence of the Cu deposition rate on the scanning speed of the laser beam, no. of scans, laser power and the temp. of the soln. were examd. More chem. reactions were running parallel during the direct writing process yielding **metallic Cu** and **Cu**(II)-oxide on the PI surface.

IT Films
Films
(**elec. conductive**; reaction dynamics of CW Ar+ laser induced copper direct writing from liq. electrolyte on **polyimide** substrates)

IT Coating process
(electroless; reaction dynamics of CW Ar+ laser induced copper direct writing from liq. electrolyte on **polyimide** substrates)

IT Electric conductors
Electric conductors
(films; reaction dynamics of CW Ar+ laser induced copper direct writing from liq. electrolyte on **polyimide** substrates)

IT Coating process
(laser-induced; reaction dynamics of CW Ar+ laser induced copper direct writing from liq. electrolyte on **polyimide** substrates)

IT Vapor deposition process
(metalization; reaction dynamics of CW Ar+ laser induced copper direct writing from liq. electrolyte on **polyimide** substrates)

IT Decomposition kinetics
Electrolytic solutions
Integrated circuits
Printed circuits
(reaction dynamics of CW Ar+ laser induced copper direct writing from liq. electrolyte on **polyimide** substrates)

IT **Polyimides**, miscellaneous

RL: MSC (Miscellaneous)
(reaction dynamics of CW Ar+ laser induced copper direct writing from liq. electrolyte on **polyimide** substrates)

IT 50-00-0, Formaldehyde, processes 1310-73-2, Sodium hydroxide (NaOH), processes 7758-98-7, Copper sulfate (CuSO4), processes 15490-42-3, Tartaric acid, potassium sodium salt, processes
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(reaction dynamics of CW Ar+ laser induced copper direct writing from liq. electrolyte on **polyimide** substrates)

IT 7440-50-8, Copper, processes
RL: PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(reaction dynamics of CW Ar+ laser induced copper direct writing from liq. electrolyte on **polyimide** substrates)

RE.CNT 19 THERE ARE 19 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L68 ANSWER 17 OF 46 HCAPLUS COPYRIGHT 2003 ACS
AN 2000:358098 HCAPLUS
DN 133:66594
TI Measurement of copper drift in methylsilsesquiazane-methylsilsesquioxane dielectric films
AU Mukaigawa, Seiji; Aoki, Tomoko; Shimizu, Yasuo; Kikkawa, Takamaro
CS Research Center for Nanodevices and Systems, Hiroshima University, Higashi-Hiroshima City, 739-8527, Japan
SO Japanese Journal of Applied Physics, Part 1: Regular Papers, Short Notes & Review Papers (2000), 39(4B), 2189-2193
CODEN: JAPNDE; ISSN: 0021-4922
PB Japanese Journal of Applied Physics
DT Journal
LA English
AB Measurement of Cu drifts in methylsilsesquiazane-methylsilsesquioxane dielec. films in the presence of an **elec.** field was **conducted** using bias-temp. stress (BTS) and capacitor-voltage (CV) anal. as well as time dependent dielec. breakdown (TDDB) stress. The amt. of Cu ions in the dielec. films can be estd. making use of the flatband voltage shift .DELTA.VFB from the BTS. Comparing the flatband voltage measured by CV anal. with the leakage current integrated over time, it is found that the main content of the leakage current during BTS is ionic current that can be attributed to the drift of Cu and mobile ions. The Cu ions cause the leakage current during TDDB stress to increase. The drift rate of Cu in methylsilsesquioxane is lower than the reported values in polyarylene ether (PAE) and fluorinated **polyimide** (FPI), and larger than that in plasma enhanced chem. vapor deposition (PECVD)-SiON.

IT Silsesquioxanes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(Me; copper drift in methylsilsesquiazane-methylsilsesquioxane dielec. films)

IT Dielectric **films**
Electric capacitance-potential relationship
Electrodiffusion
Integrated circuits
Leakage current
(**copper** drift in methylsilsesquiazane-methylsilsesquioxane dielec. films)

IT Electric current
(ionic; copper drift in methylsilsesquiazane-methylsilsesquioxane dielec. films)

IT Silazanes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(silsesquiazanes, Me; copper drift in methylsilsesquiazane-methylsilsesquioxane dielec. films)

IT 7440-50-8, Copper, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(copper drift in methylsilsesquiazane-methylsilsesquioxane dielec. films)

RE.CNT 10 THERE ARE 10 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L68 ANSWER 18 OF 46 HCAPLUS COPYRIGHT 2003 ACS
AN 2000:307073 HCAPLUS
DN 132:300116
TI Method of fabricating coated powder materials and their use for high conductivity paste applications
IN Kang, Sung Kwon; Purushothaman, Sampath; Rai, Rajinder Singh
PA International Business Machines Corporation, USA
SO U.S., 19 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6059952	A	20000509	US 1998-111155	19980707
PRAI	US 1997-52172P	P	19970710		

AB Methods for forming pastes of powder particles coated with an **elec**. **conductive** coating are described. The powder particles, with or without an optional first conductive coating layer applied to their surface, are placed in contact with a cathode surface and immersed in an electroplating soln. An anode covered with a nonconducting but ion-permeable membrane is immersed in the soln. in close proximity to the cathode. Agitation to move and gently tumble the powder over the cathode surface is provided. The powder particles are plated with a metal or metal alloy coating by biasing the anode with a pos. voltage relative to the cathode. The coated powder is removed, rinsed and dried. The powder is added to a polymer material to form a paste which is heated to fuse the powder coating surfaces to form a network of interconnected particles and is further heated to cure the polymer. When the paste is disposed between adjacent **elec**. **conductive** surfaces, the coated particles fuse to the **elec**. **conductive** surfaces to form elec. interconnections.

IT Electric potential
(biasing during tin-bismuth alloy electrodeposition on copper powder in fabricating conducting paste from tin **coated copper** powder and polymer)

IT Electric conductors
Electrical materials
Electrically conductive pastes
Electrodeposition
Powders
(fabricating coated powder materials and their use for high cond. paste applications)

IT **Microelectronics**
Printed circuit boards
(fabricating coated powder materials and their use for high cond. paste applications, in)

use for high cond. paste applications)
IT 57-55-6, 1,2-Propanediol, uses 79-20-9, Methyl acetate 93-58-3, Methyl benzoate 93-89-0, Ethyl benzoate 98-86-2, Acetophenone, uses 872-50-4, uses
RL: NUU (Other use, unclassified); PRP (Properties); USES (Uses)
(use as solvent in fabricating coated powder materials for high cond. paste applications)
RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L68 ANSWER 19 OF 46 HCAPLUS COPYRIGHT 2003 ACS
AN 2000:31236 HCAPLUS
DN 132:101413
TI Coatings for EMI/RFI shielding
IN Paneccasio, Vincent, Jr.; Chasse, Mark P.
PA Enthone-Omi, Inc., USA
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6013203	A	20000111	US 1998-136219	19980819
	WO 2000011681	A1	20000302	WO 1999-US17070	19990728
	W: CA, CN, JP, KR				
	RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
	US 6375866	B1	20020423	US 2000-478951	20000107
PRAI	US 1998-136219	A	19980819		

AB An **elec. conductive** paint for providing EMI/RFI shielding for housings of electronic components comprises a crosslinked org. resin binder contg. crosslinkable functional groups such as OH groups, **elec. conductive** metallic particles, preferably a mixt. of Ag flakes and Ag-**coated Cu** flakes, a solvent, a crosslinking agent which crosslinks with itself and with the functional groups of the org. binder, and preferably a catalyst which accelerates crosslinking of the crosslinking agent and org. binder. Using such a paint formulation, it has been found that thinner coatings can be used while still exceeding the properties needed for EMI/RFI shielding of housings for electronic components. A rheol. additive which is an org. deriv. of castor oil is preferably used to control the viscosity and spraying characteristics of the paint, esp. in a paint compn. contg. Ag-**coated Cu** flakes. The conductive paint provides a sprayed coating which is durable, has low resistivity, is smooth, and has both cohesive and adhesive strength. A method is also provided for forming EMI/RFI shielding on housings for electronic components and electronic components made using the method and paint compn. of the invention.
IT Polymers, uses
RL: TEM (Technical or engineered material use); USES (Uses)
(binders; coatings for emi/RFI shielding of electronic components contg.)
IT Electric apparatus
Microelectronic devices
(coatings for emi/RFI shielding of)
IT Electromagnetic shields
(coatings for emi/RFI shielding of electronic components)
IT Catalysts
Crosslinking agents
(coatings for emi/RFI shielding of electronic components contg.)

IT Paints
(for emi/RFI shielding of electronic components)
IT Spraying
(of coatings for emi/RFI shielding of electronic components)
IT Binders
(**polymeric**; coatings for emi/RFI shielding of electronic components contg.)
IT 139-44-6
RL: MOA (Modifier or additive use); TEM (Technical or engineered material use); USES (Uses)
(Thixcin R, rheol. additive; coatings for emi/RFI shielding of electronic components contg.)
IT 7440-22-4, Silver, uses 7440-50-8, **Copper**, uses
RL: TEM (Technical or engineered material use); USES (Uses)
(**coatings** for emi/RFI shielding of electronic components contg.)
IT 254436-04-9, Thixatrol Plus
RL: MOA (Modifier or additive use); TEM (Technical or engineered material use); USES (Uses)
(rheol. additive; coatings for emi/RFI shielding of electronic components contg.)
RE.CNT 12 THERE ARE 12 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L68 ANSWER 20 OF 46 HCAPLUS COPYRIGHT 2003 ACS
AN 1999:236552 HCAPLUS
DN 130:283165
TI **Polyimide**-based thickness-direction **electrically conductive** sheets with good conduction reliability and manufacturing methods therefor
IN Takeuchi, Etsu; Okukawa, Yoshitaka
PA Sumitomo Bakelite Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 11 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 11100444	A2	19990413	JP 1997-264255	19970929
PRAI JP 1997-264255		19970929		

AB Sheets comprise (i) **polyimides** prepd. from (a) H2NR5(SiR1R2O)kSiR3R4R6NH2 (R1-4 = H, C.ltoreq.6 hydrocarbyl; R5, R6 = C1-6 bivalent hydrocarbyl; k = 4-10), (b) 2,2-bis[4-(4-aminophenoxy)phenyl]propane (I), 2,2-bis[4-(4-aminophenoxy)phenyl]hexafluoropropane, bis[4-(4-aminophenoxy)phenyl]ether, 1,3-bis(3-aminophenoxy)benzene (II), 1,4-bis(3-aminophenoxy)benzene, 1,4-bis(4-aminophenoxy)benzene, 3,4'-diaminodiphenyl ether, 2,5-diamino-p-xylene, and/or 1,3-bis(3-aminopropyl)-1,1,3,3-tetramethyldisiloxane, (c) diamines excluding (b), (d) 4,4'-oxydiphthalic acid dianhydride (III), 3,3',4,4'-biphenyltetracarboxylic acid dianhydride, and/or 3,3',4,4'-benzophenonetetracarboxylic acid dianhydride, and (e) acid dianhydrides excluding (d) at (a)/[(a) + (b) + (c)] 0.1-0.5 (mol ratio), (b)/[(a) + (b) + (c)] 0.5-0.9, (d)/[(d) + (e)] 0.8-1, and [(d) + (e)]/[(a) + (b) + (c) + (d) + (e)] 0.9-1.1 (mol ratio) and (ii) (isolated) contact terminals arranged on one or both sides of (i). A manufg. process for the sheets includes photolithog. to form (isolated) contact terminals on one or both sides of the **polyimide** sheets. Thus, a **Cu** foil was **coated** with a soln. of 78.9:15.6:31.0:29.3 II-I-III-.alpha.,.omega.-bis(3-aminopropyl)dimethylsiloxane copolymer and etched via a resist mask to

give a flexible anisotropic conductive sheet, which was hot pressed with a semiconductor-mounting tape to give a semiconductor package showing good reliability of **elec. conduction** and adhesion between **chip** electrodes and contact terminals.

IT Photolithography
Semiconductor materials
(anisotropic electroconductive sheets comprising **polyimide**-polysiloxanes for flip-**chip** bonding of semiconductor **chips**)

IT Electric conductors
Electric conductors
(anisotropic, sheets; anisotropic electroconductive sheets comprising **polyimide**-polysiloxanes for flip-**chip** bonding)

IT Anisotropic materials
Anisotropic materials
(**elec. conductors**, sheets; anisotropic electroconductive sheets comprising **polyimide**-polysiloxanes for flip-**chip** bonding)

IT Polysiloxanes, uses
Polysiloxanes, uses
RL: IMF (Industrial manufacture); PRP (Properties); TEM (Technical or engineered material use); PREP (Preparation); USES (Uses)
(**polyimide**-; anisotropic electroconductive sheets comprising **polyimide**-polysiloxanes for flip-**chip** bonding of semiconductor **chips**)

IT **Polyimides**, uses
Polyimides, uses
RL: IMF (Industrial manufacture); PRP (Properties); TEM (Technical or engineered material use); PREP (Preparation); USES (Uses)
(polysiloxane-; anisotropic electroconductive sheets comprising **polyimide**-polysiloxanes for flip-**chip** bonding of semiconductor **chips**)

IT 156551-00-7P 159354-13-9P
RL: DEV (Device component use); IMF (Industrial manufacture); PRP (Properties); PREP (Preparation); USES (Uses)
(anisotropic electroconductive sheets comprising **polyimide**-polysiloxanes for flip-**chip** bonding of semiconductor **chips**)

IT 7440-50-8, Copper, uses
RL: DEV (Device component use); USES (Uses)
(contact; anisotropic electroconductive sheets comprising **polyimide**-polysiloxanes for flip-**chip** bonding of semiconductor **chips**)

L68 ANSWER 21 OF 46 HCAPLUS COPYRIGHT 2003 ACS
AN 1999:165545 HCAPLUS
DN 130:312731
TI Development of low-cost, low-temperature conductive adhesives
AU Kang, Sung K.; Purushothaman, S.
CS IBM Research Division, T.J. Watson Research Center, Yorktown Heights, NY, 10598, USA
SO Proceedings - Electronic Components & Technology Conference (1998), 48th, 1031-1035
CODEN: PETCES
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
AB Elec. and/or thermally conductive materials comprising metallic filler particles and polymer matrix have been actively investigated as replacements for the solder interconnections used in **microelectronic** applications. Silver-filled epoxy resin materials

originally developed for thermal conduction in **die** attach applications have been candidates for this purpose. However, several limitations have been realized when they are considered as a replacement for solder interconnections, such as low **elec. cond.**, low joint strength, increase in contact resistance upon thermal cycling, lack of reworkability, and silver migration. In order to overcome these limitations, a new formulation has been developed based on alternative high conducting filler particles and tailored polymer resins. The high conducting filler particles are coated with low m.p., non-toxic metals or alloys which can be fused to achieve metallurgical bonding between adjacent particles as well as particles to the substrate contacts. Specifically, an **elec. conductive** adhesive made of Sn-**coated Cu** powder and **polyimide** siloxane resin was developed, and their salient properties were reported previously. This material is a good candidate for the high temp. solder joints such as controlled collapse **chip** connection (C4) and solder ball connection (SBC) to a ceramic substrate, but not for the **polymeric** printed circuit board applications. In this paper, we report a new formulation of **elec. conductive** adhesive materials with coated metal filler, which can be used for low temp. as well as low cost applications.

IT Adhesives
(conductive; development and formulation of low-cost, low-temp. **conductive** adhesives for **elec.** circuit application)

IT Printed circuit boards
(development and formulation of low-cost, low-temp. **conductive** adhesives for **elec.** circuit application)

IT Metals, uses
RL: DEV (Device component use); MOA (Modifier or additive use); USES (Uses)
(development and formulation of low-cost, low-temp. **conductive** adhesives for **elec.** circuit application)

IT Polysiloxanes, uses
Polysiloxanes, uses
RL: DEV (Device component use); POF (Polymer in formulation); USES (Uses)
(**polyimide**-; development and formulation of low-cost, low-temp. **conductive** adhesives for **elec.** circuit application)

IT **Polyimides**, uses
Polyimides, uses
RL: DEV (Device component use); POF (Polymer in formulation); USES (Uses)
(polysiloxane-; development and formulation of low-cost, low-temp. **conductive** adhesives for **elec.** circuit application)

IT 7440-31-5, Tin, uses 7440-50-8, Copper, uses
RL: DEV (Device component use); MOA (Modifier or additive use); USES (Uses)
(development and formulation of low-cost, low-temp. **conductive** adhesives for **elec.** circuit application)

RE.CNT 23 THERE ARE 23 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L68 ANSWER 22 OF 46 HCAPLUS COPYRIGHT 2003 ACS
AN 1999:137427 HCAPLUS
DN 130:161738
TI Manufacture of multilayer circuits using photosensitive dielectric organics
IN Flacker, Alexander; Gozzi, Antonio Cezar; Dos Santos, Maria Felomena Cassia de Jesus; Zucolo, Ana Cecilia Pagotto; Marini de Almeida, Antonio; Barnett, Moacir
PA Telecumunicacoes Brasileiras S/A - Telebras, Brazil
SO Braz. Pedido PI, 38 pp.

CODEN: BPXXDX
DT Patent
LA Portuguese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	BR 9600574	A	19971230	BR 1996-574	19960214
PRAI	BR 1996-574		19960214		

AB The method, comprising a 1st level of **elec. conductive** metallic tracks deposited on an Al2O3 substrate and by .gtoreq.1 addnl. **elec. conductive** metallic tracks deposited on, but sepd. from the 1st level by an imidized polyamic ester layer, and the surface of which was subjected to a drying process to improve adhesion of the metals, a reactive O plasma is applied to sensitize, activate the surface, and deposit on the surface, by electroless deposition, a 1st metallic layer contg. Ni as main component, e.g., Ni-P, Ni-B, and a Ni layer by electrolysis. The electroless deposition process is followed by a heat treatment at 100-200.degree. in flowing N. This process is esp. suitable for producing high-d. multichip modules on ceramic supports. Rubalit 708 (.alpha.-Al2O3) supports (purity 96%; roughness 0.25-0.34 .mu.m) were extensively cleaned, sensitized with SnCl2 and PdCl2, coated with Ni by electroless deposition using a electroless deposition soln. of 70.degree. contg. NiCl2 12.5, dimethylamine borane 1.6, and di-Na tartrate 47.2 g/L while treating the soln. with ultrasound for 30 s, coated with Ni by electrolysis to thickness .apprx.0.7 .mu.m using a Deweka 720 (Ni soln.), washed, **coated** with **Cu** by electrolysis using Copper Clean PCM (Cu soln. contg. CuSO4 75-90, H2SO4 187.5 g/L, and chloride 75 ppm), coated by electrolysis with Ni, coated with S 1400/26 (photoresist), exposed to AZ 351, etching the metal coatings, activating the photoresist, coated with Pyralin P.I.2700 (**polyimide**) 2nd layer, exposed to DE 6018, the **polyimide** cured, treated with O plasma, electroless coated with N-P using a soln. contg. NiSO4.bul.6H2O 26, Na3C6H5O7.bul.6H2O 56, NaH2PO2.bul.H2O 17, and (NH4)2SO4 66 g/L, heat-treated in flowing N, immersed in 10% H2SO4, coated with Ni by electrolysis, washed, coated with Ni by electrolysis, and, optionally, with Au.

IT Photoresists
(coating with, electroless; of photosensitive **polyimide**-coated ceramic supports, in high-d. multilayer **chip** manuf.)

IT Coating process
(electroless, of ceramic supports; with nickel-phosphorus, for photosensitive **polyimide** coating formation in high-d. multilayer **chip** manuf.)

IT Heat treatment
(in nitrogen; for adhesion of metallic coating to photosensitive **polyimide**-coated ceramic supports in high-d. multilayer **chip** manuf.)

IT Printed circuits
(multilayer; photosensitive **polyimide**-coated ceramic support manuf. for)

IT Electrodeposition
(of ceramic supports; with nickel, for photosensitive **polyimide** coating formation in high-d. multilayer **chip** manuf.)

IT Coating process
(of ceramic supports; with photosensitive **polyimide**, in high-d. multilayer **chip** manuf.)

IT Electronic device fabrication
(of photosensitive **polyimide**-coated ceramic supports in high-d. multilayer **chip** manuf.)

IT **Polyimides**, uses
RL: TEM (Technical or engineered material use); USES (Uses)
(photosensitive, coating with; of ceramic supports, in high-d.

multilayer **chip** manuf.)
IT Light-sensitive materials
(**polyimides**, coating with; in high-d. multilayer **chip** manuf.)
IT Ceramics
(supports, coating of; with photosensitive dielec. **polyimide**, in high-d. multilayer **chip** manuf.)
IT 31942-21-9
RL: TEM (Technical or engineered material use); USES (Uses)
(Pyralin PI 2700, photosensitive **polyimide**, coating with; of ceramic supports, in high-d. multilayer **chip** manuf.)
IT 11143-14-9 11146-55-7
RL: TEM (Technical or engineered material use); USES (Uses)
(coating with, electroless; of ceramic supports, for photosensitive **polyimide** coating formation in high-d. multilayer **chip** manuf.)
IT 7440-57-5, Gold, uses
RL: TEM (Technical or engineered material use); USES (Uses)
(**coating** with; of **copper** and nickel **coating** on photosensitive **polyimide** coating on ceramic supports, in high-d. multilayer **chip** manuf.)
IT 7440-50-8, Copper, uses
RL: TEM (Technical or engineered material use); USES (Uses)
(electroplating with; of nickel coating on photosensitive **polyimide** coating on ceramic supports, in high-d. multilayer **chip** manuf.)
IT 7440-02-0, Nickel, uses
RL: TEM (Technical or engineered material use); USES (Uses)
(electroplating with; of nickel-phosporus coating on ceramic supports, for photosensitive **polyimide** coating formation in high-d. multilayer **chip** manuf.)
IT 7727-37-9, Nitrogen, uses
RL: NUU (Other use, unclassified); USES (Uses)
(heat-treating in; for adhesion of metallic coating to photosensitive **polyimide**-coated ceramic supports, in high-d. multilayer **chip** manuf.)
IT 7782-44-7, Oxygen, uses
RL: NUU (Other use, unclassified); USES (Uses)
(plasma; in photosensitive **polyimide**-coated ceramic support formation on ceramics supports in high-d. multilayer **chip** manuf.)
IT 1344-28-1, Alumina, uses
RL: TEM (Technical or engineered material use); USES (Uses)
(.alpha.-, Rubalit 708, supports, coating of; with photosensitive dielec. **polyimide**, in high-d. multilayer **chip** manuf.)

L68 ANSWER 23 OF 46 HCAPLUS COPYRIGHT 2003 ACS
AN 1999:114398 HCAPLUS
DN 130:161737
TI Electric conductive paste structure and its manufacture
IN Jerome, Jeffrey; Kang, Sung Kwon; Purushothaman, Sampath
PA International Business Machines Corp., USA
SO Jpn. Kokai Tokkyo Koho, 12 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 11045618	A2	19990216	JP 1998-160246	19980609

US 6238599 B1 20010529 US 1997-877991 19970618
PRAI US 1997-877991 A 19970618

AB The structure has a resin selected from .gtoreq.1 of a phenoxy polymer and a a styrene-allyl alc.-based resin in which several particles having **elec. conductive** coating films are dispersed, in which the particles can be adhered via the films. The structure has binded particle-based networks having spaces comprising a phenoxy polymer and a styrene-allyl alc.-based resin, in which each particle has a heat-meltable material-based coating film and adjacent particles inside the networks can be adhered by the material. The structure contains a resin mixt. comprising a phenoxy polymer, a styrene-allyl alc.-based resin, and a flux agent and **Cu** powders **coated** with a material contg. Sn, In, Bi, Sb, and/or their mixt. The manuf. method involves (1) prepg. a paste comprising a polymer material comprising a phenoxy polymer and a styrene-allyl alc.-based resin in which **elec. conductive** film-contg. particles are dispersed, (2) applying the paste between a 1st **elec. conductive** face and a 2nd **elec. conductive** face, (3) heating the paste to form the network comprising the particles, and (4) heat-curing the polymer material. The method gives an environmental friendly **elec. conductive** paste with high **elec. cond.** at low cost. The paste is useful for an **integrated circuit**, a high-d. printed circuit board, etc.

IT **Electrically conductive** pastes
Integrated circuits
Printed circuits
(manuf. of environmental friendly **elec. conductive** paste structure)

IT **Polyimides**, uses
Polysiloxanes, uses
RL: DEV (Device component use); USES (Uses)
(manuf. of environmental friendly **elec. conductive** paste structure)

IT Phenoxy resins
RL: DEV (Device component use); MOA (Modifier or additive use); USES (Uses)
(manuf. of environmental friendly **elec. conductive** paste structure)

IT Polysiloxanes, uses
Polysiloxanes, uses
RL: DEV (Device component use); USES (Uses)
(**polyimide-**; manuf. of environmental friendly **elec. conductive** paste structure)

IT **Polyimides**, uses
Polyimides, uses
RL: DEV (Device component use); USES (Uses)
(polysiloxane-; manuf. of environmental friendly **elec. conductive** paste structure)

IT 7429-90-5, Aluminum, uses 7440-05-3, Palladium, uses 7440-06-4, Platinum, uses 7440-22-4, Silver, uses 7440-50-8, Copper, uses 7440-57-5, Gold, uses 9004-34-6, Cellulose, uses **9005-53-2**, Lignin, uses
RL: DEV (Device component use); USES (Uses)
(manuf. of environmental friendly **elec. conductive** paste structure)

IT 25068-38-6, Bisphenol A-epichlorohydrin copolymer 25119-62-4, Allyl alcohol-styrene copolymer
RL: DEV (Device component use); MOA (Modifier or additive use); USES (Uses)
(manuf. of environmental friendly **elec. conductive** paste structure)

IT 7439-92-1, Lead, uses 7440-31-5, Tin, uses 7440-36-0, Antimony, uses 7440-66-6, Zinc, uses 7440-69-9, Bismuth, uses 7440-74-6, Indium, uses
RL: DEV (Device component use); TEM (Technical or engineered material use); USES (Uses)
(manuf. of environmental friendly **elec. conductive** paste structure)

L68 ANSWER 24 OF 46 HCAPLUS COPYRIGHT 2003 ACS
AN 1999:34632 HCAPLUS
DN 130:140232
TI Flexible circuit boards with good punchability and peel strength
IN Inoue, Hiroshi; Ohtani, Akinori; Ano, Hiroshi
PA Ube Industries, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 10 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 11004055	A2	19990106	JP 1998-19060	19980130
PRAI	JP 1997-101532		19970418		

AB The circuit boards comprise an **elec. conductor** and an arom. **polyimide** film with thickness 10-125 .mu.m, sp. end tear strength (SETS) 11-22 kg/20 mm/10 .mu.m, and volatiles content .ltoreq.0.4%. Prepg. a polyamic acid of 3,3',4,4'-biphenyltetracarboxylic dianhydride-p-phenylenediamine copolymer in AcNMe2, extruding through a T-**die**, treating the resulting film with aminosilane, and curing at 240.degree. gave a **polyimide** film with thickness 25 .mu.m, SETS 13.2, and volatiles content 0.13%. The film was coated with a thermosetting adhesive, roll laminated with a Cu foil, hot pressed, and patterned to give a flexible circuit board with good punchability and peel strength 2.1 kg/cm at 180.degree..

IT **Polyimides**, uses
RL: TEM (Technical or engineered material use); USES (Uses)
(film laminate; flexible circuit boards with good punchability and peel strength)

IT Printed circuit boards
(flexible; flexible circuit boards with good punchability and peel strength)

IT Polysiloxanes, uses
Polysiloxanes, uses
RL: TEM (Technical or engineered material use); USES (Uses)
(**polyimide-**, epoxy resin, adhesives; flexible circuit boards with good punchability and peel strength)

IT **Polyimides**, uses
Polyimides, uses
RL: TEM (Technical or engineered material use); USES (Uses)
(polysiloxane-, epoxy resin, adhesives; flexible circuit boards with good punchability and peel strength)

IT Adhesives
(thermosetting, **polyimide**-siloxane-epoxy resin; flexible circuit boards with good punchability and peel strength)

IT 219982-39-5P, 2,3,3',4'-Biphenyltetracarboxylic dianhydride-aminopropyl-terminated di-methyl siloxane-2,2-bis[4-(4-aminophenoxy)phenyl]propane-Epikote 807-ELM 100-H5 copolymer
RL: IMF (Industrial manufacture); TEM (Technical or engineered material use); PREP (Preparation); USES (Uses)
(adhesive; flexible circuit boards with good punchability and peel strength)

IT **29319-22-0P**, 3,3',4,4'-Biphenyltetracarboxylic

dianhydride-p-phenylenediamine copolymer
RL: IMF (Industrial manufacture); TEM (Technical or engineered material use); PREP (Preparation); USES (Uses)
(**film**, **copper** laminate; flexible circuit boards with good punchability and peel strength)

IT **32197-39-0P**, 3,3',4,4'-Biphenyltetracarboxylic dianhydride-p-phenylenediamine copolymer, sru 71329-95-8P, 3,3',4,4'-Biphenyltetracarboxylic dianhydride-p-phenylenediamine copolymer, sru
RL: IMF (Industrial manufacture); TEM (Technical or engineered material use); PREP (Preparation); USES (Uses)
(flexible circuit boards with good punchability and peel strength)

IT 7440-50-8P, Copper, uses
RL: IMF (Industrial manufacture); TEM (Technical or engineered material use); PREP (Preparation); USES (Uses)
(foil, **polyimide** film laminate; flexible circuit boards with good punchability and peel strength)

L68 ANSWER 25 OF 46 HCAPLUS COPYRIGHT 2003 ACS
AN 1998:813642 HCAPLUS
DN 130:89398
TI Metallic-conductor/**polyimide**-dielectric multilayer assembly having gas-discharging holes for multichip modules
IN Takahashi, Yasuhito; Beilin, Solomon I.; Peters, Michael G.
PA Fujitsu Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 10 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 10335535	A2	19981218	JP 1998-137075	19980519
	US 6106923	A	20000822	US 1997-859642	19970520
PRAI	US 1997-859642	A	19970520		

AB The multilayer assembly is alternately laminated body with **Cu layers** and **polyimide** dielec. layers and has gas-discharging holes to the metallic layers on the ground plane. The assembly provides discharging of gas trapped in the dielec. layers without interacting the function of the a.c. plane which provides controlling impedance characteristics in the signal wires.

IT Electric impedance
(controlling wires; metallic-conductor/**polyimide**-dielec. multilayer assembly having gas-discharging holes for multichip modules)

IT **Polyimides**, properties
RL: DEV (Device component use); PRP (Properties); TEM (Technical or engineered material use); USES (Uses)
(dielec. material; metallic-conductor/**polyimide**-dielec. multilayer assembly having gas-discharging holes for multichip modules)

IT Electric insulators
(metallic-conductor/**polyimide**-dielec. multilayer assembly having gas-discharging holes for multichip modules)

IT Multilayers
(metallic-conductor/**polyimide**-dielec.; metallic-conductor/**polyimide**-dielec. multilayer assembly having gas-discharging holes for multichip modules)

IT Electric conductors
(metallic; metallic-conductor/**polyimide**-dielec. multilayer assembly having gas-discharging holes for multichip modules)

IT **Integrated circuits**
(multichip modules; metallic-conductor/**polyimide**-dielec.

multilayer assembly having gas-discharging holes for multichip modules)

IT 7440-50-8, Copper, properties
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PRP (Properties); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(**elec. conductors**; metallic-**conductor**/ **polyimide**-dielec. multilayer assembly having gas-discharging holes for multichip modules)

L68 ANSWER 26 OF 46 HCAPLUS COPYRIGHT 2003 ACS
AN 1998:402259 HCAPLUS
DN 129:102879
TI Stacking of thin metal films for controlled collapse chipconnection and structure thereof
IN Kaja, Suryanarayana; Perfecto, Eric D.; Prasad, Chandrika; Rufing, Kim H.; Totta, Paul A.
PA International Business Machines Corp., USA
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 10163590	A2	19980619	JP 1997-290703	19971023
PRAI US 1996-752470		19961119		

AB The title process comprises prepn. of a metal base layer(e.g., contg. an adhesion layer from Cr, Ti, Ta, Zr, Hf, and/or Mo, and an **elec. conductive layer** from **Cu** and/or Al on the adhesion layer) on a substrate, and sequential lamination of a Ni, a Au, a Ni, and a Au layer on the metal base layer (e.g., a **polyimide** passivation film may be placed on the 2nd Au layer orbefore lamination of the 2nd Au layer to limit the region of the 2nd Au layer) for solder bonding of **integrated circuit chips** and substrates. No damage of connection by reflow of a solder is found and wet etching of the seed layer of the metal base layer is made possible with the Au layers.

IT Electric contacts
(controlled collapse **chip** connection with nickel-gold alternate laminates on metal base layers)

IT Soldering
(for controlled collapse **chip** connection with nickel-gold alternate laminates on metal base layers)

IT **Polyimides**, properties
RL: PRP (Properties); TEM (Technical or engineered material use); USES (Uses)
(for passivation films on nickel-gold aternate laminates for controlled collapse **chip** connection)

IT Electronic packaging materials
(nickel-gold alternate laminate on metal base layers for controlled collapse **chip** connection)

IT 7440-47-3, Chromium, processes 7440-50-8, **Copper**, processes
RL: PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(**film**; for metal base layers on substrates of nickel-gold alternate laminates for controlled collapse **chip** connection)

IT 7440-57-5, Gold, processes
RL: PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(film; nickel-gold alternate laminate on metal base layers for controlled collapse **chip** connection)

IT 7440-02-0, Nickel, processes
RL: PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(nickel-gold alternate laminate on metal base layers for controlled collapse **chip** connection)

L68 ANSWER 27 OF 46 HCAPLUS COPYRIGHT 2003 ACS
AN 1997:226106 HCAPLUS
DN 126:219557
TI Semiconductor device, its manufacture, and probe card using it
IN Shimada, Juzo; Senba, Naoharu; Takahashi, Nobuaki
PA Nippon Electric Co, Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 09036122	A2	19970207	JP 1995-186022	19950721
	US 5793117	A	19980811	US 1996-684617	19960722
PRAI	JP 1995-186022		19950721		

AB The device comprises a p- or n-type Si or GaAs substrate and a pit part having an **elec. conducting** layer and a ball bump. The device is manufd. by applying a resist on a semiconductor **wafer**, exposing, developing, etching to form a pit part, forming a metal oxide layer, a contact hole, an **elec. conducting** layer, and a protective film, forming a thin-film **elec. conducting layer** comprising Ti/**Cu**, Ni/Au, or Cr/Cu/Au, and heating to form a ball bump. The probe card comprises the device. The ball bump showed good adhesion strength.

IT Brazes
(ball bump; semiconductor device having probe card, its manuf., and probe card using it)

IT **Polyimides**, uses
RL: DEV (Device component use); USES (Uses)
(protective film; semiconductor device having probe card, its manuf., and probe card using it)

IT Semiconductor devices
(semiconductor device having probe card, its manuf., and probe card using it)

IT 7440-74-6, Indium, uses 11110-87-5 11125-88-5 11144-61-9
RL: DEV (Device component use); USES (Uses)
(ball bump; semiconductor device having probe card, its manuf., and probe card using it)

IT 7429-90-5, Aluminum, uses 7440-02-0, Nickel, uses 7440-21-3, Silicon, uses 7440-32-6, Titanium, uses 7440-47-3, Chromium, uses 7440-50-8, Copper, uses 7440-57-5, Gold, uses 7631-86-9, Silicon oxide, uses
RL: DEV (Device component use); USES (Uses)
(semiconductor device having probe card, its manuf., and probe card using it)

L68 ANSWER 28 OF 46 HCAPLUS COPYRIGHT 2003 ACS
AN 1997:102051 HCAPLUS
DN 126:147170
TI Vacuum-chamber apparatus for forcing of electroless coating solution into narrow openings on electric-circuit **chips**
IN Grilletto, Carlo; Love, David G.
PA Fujitsu Ltd., Japan
SO U.S., 7 pp.
CODEN: USXXAM

DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5597412	A	19970128	US 1995-388998	19950215
PRAI	US 1995-388998		19950215		

AB The **chip** and module substrates having narrow grooves on the surface to be filled with **elec. conductor** metal are selectively coated in a sealable vacuum chamber using a pressurized electroless soln. forced into the slits. The chamber app. is optionally divided by a flexible wall, and the coating soln. in the loaded subchamber is pressurized by applying compressed air into the other subchamber to develop hydrostatic pressure across the flexible wall. The microgrooves 10-40 .mu.m wide in a **polyimide film** on **Cu** substrate can be filled with a metal from electroless bath forced into the microgrooves.

IT **Integrated circuits**
(coating on; vacuum-chamber app. for electroless metal coating in grooves on elec.-circuit **chips**)

IT Coating process
(electroless, in grooves; vacuum-chamber app. for electroless metal coating in grooves on elec.-circuit **chips**)

IT **Polyimides**, processes
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(film, coating of; vacuum-chamber app. for electroless metal coating in grooves on elec.-circuit **chips**)

IT 7440-50-8, **Copper**, processes
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(**coating** with, in grooves; vacuum-chamber app. for electroless metal coating in grooves on elec.-circuit **chips**)

L68 ANSWER 29 OF 46 HCAPLUS COPYRIGHT 2003 ACS
AN 1997:93984 HCAPLUS
DN 126:111879
TI Thick-film conductive paste composition
IN Inaba, Akira; Kuno, Hideoki
PA E.I. Du Pont De Nemours and Company, USA
SO Eur. Pat. Appl., 8 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 747912	A2	19961211	EP 1996-108829	19960603
	R: DE, FR, GB				
	JP 08329736	A2	19961213	JP 1995-160123	19950605
	CN 1149191	A	19970507	CN 1996-110427	19960605
PRAI	JP 1995-160123		19950605		

AB This invention is directed to a thick-film conductive paste compn. comprising a conductive paste, a polymer binder, and .gtoreq.1 org. additive (an amidosulfuric acid metal salt, a higher fatty acid metal salt, and/or a metal resinate) used for forming the terminations of **chip** resistors without occurrence of swelling and/or cracks in the superimposed area of the termination and resistor.

IT Resistors
(**chip**; thick-film conductive paste compns. for terminations of)

IT Fatty acids, uses
RL: DEV (Device component use); TEM (Technical or engineered material

use); USES (Uses)
(metal salts; thick-film conductive paste compns. contg.)
IT Binders
(**polymeric**; thick-film conductive paste compns. contg.)
IT Resin acids
RL: DEV (Device component use); TEM (Technical or engineered material use); USES (Uses)
(salts; thick-film conductive paste compns. contg.)
IT **Electrically conductive** pastes
(thick-film conductive paste compn. for **chip** resistor terminations)
IT Frits
(thick-film conductive paste compns. contg.)
IT Electric conductors
(thick-film pastes for **chip** resistor terminations)
IT 557-05-1, Zinc stearate 637-12-7, Aluminum stearate 1592-23-0, Calcium stearate 7440-05-3, Palladium, uses 7440-22-4, Silver, uses 7617-31-4, **Copper** stearate 13586-84-0, Cobalt stearate
RL: DEV (Device component use); TEM (Technical or engineered material use); USES (Uses)
(thick-**film** conductive paste compns. contg.)

L68 ANSWER 30 OF 46 HCAPLUS COPYRIGHT 2003 ACS
AN 1996:443753 HCAPLUS
DN 125:102623
TI Formation of wiring layer
IN Ezawa, Hirokazu; Myata, Masahiro
PA Tokyo Shibaura Electric Co, Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 08111474	A2	19960430	JP 1994-243739	19941007
	JP 3243381	B2	20020107		
PRAI	JP 1994-243739		19941007		

AB The formation involves the following steps; (1) forming 1st opening (corresponding a wiring pattern) in 1st resist film formed on a substrate, (2) forming 1st metal microparticle film in the opening and on the resist film, (3) forming 2nd resist film on the 1st metal microparticle film, and then forming 2nd opening in the 2nd resist film, (4) forming a metal plating layer in the 2nd opening, (5) forming 2nd metal microparticle film on the metal layer and on 2nd resist film, and (6) removing the 1st- and 2nd resist films, and simultaneously removing the 1st- and 2nd metal microparticle films at a part excluding above the metal layer. Thus, a wiring having a core-sheath structure composed of Ti/Pd laminate film at the side and bottom of the sheath, Ni film at the top of the sheath, and Cu core was manufd. by the method. The wiring inhibits undesired effects of such as **polyimides** and SiO2 onto the **Cu layer**, and has high reliability.
IT Electric **conductors**
(**elec**. wiring layer contg. core-sheath composite structure in **integrated circuits**)
IT Electric circuits
(integrated, elec. wiring layer contg. core-sheath composite structure in **integrated circuits**)
IT 7440-02-0, Nickel, uses 7440-05-3, Palladium, uses 7440-06-4, Platinum, uses 7440-22-4, Silver, uses 7440-32-6, Titanium, uses 7440-57-5, Gold, uses

RL: DEV (Device component use); USES (Uses)
(elec. wiring layer contg. core-sheath composite structure in **integrated circuits**)
IT 7440-50-8P, Copper, uses
RL: DEV (Device component use); PNU (Preparation, unclassified); PREP (Preparation); USES (Uses)
(elec. wiring layer contg. core-sheath composite structure in **integrated circuits**)

L68 ANSWER 31 OF 46 HCAPLUS COPYRIGHT 2003 ACS
AN 1996:273399 HCAPLUS
DN 124:304240
TI Printed circuit boards
IN Kikuchi, Hideo
PA Nippon Electric Co, Japan
SO Jpn. Kokai Tokkyo Koho, 11 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 08046322	A2	19960216	JP 1994-177869	19940729
	JP 2725605	B2	19980311		
PRAI	JP 1994-177869		19940729		

AB Thin plates are laminated and through holes in the laminated plates are filled, forming boards, resins (e.g., **polyimide**) are deposited on both sides of the **wafers** except where openings are planned, openings are formed by removing the fillers, creating through holes **elec. conductors** (e.g., Cu) are plated on the boards as well as the hole inner walls, and the **elec. conductive** films are etched into interconnection patterns.
IT Epoxy resins, uses
Phenolic resins, uses
Polyimides, uses
RL: DEV (Device component use); USES (Uses)
(resin deposition for printed circuit boards)
IT Electric circuits
(printed, boards, metal deposition and patterning for)
IT 7440-50-8, **Copper**, uses
RL: DEV (Device component use); USES (Uses)
(**metal** deposition and patterning for printed circuit boards)

L68 ANSWER 32 OF 46 HCAPLUS COPYRIGHT 2003 ACS
AN 1994:669648 HCAPLUS
DN 121:269648
TI Formation of bump contacts for high-frequency semiconductor devices
IN Yanagihara, Hiroshi
PA Tanaka Precious Metal Ind, Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 06084917	A2	19940325	JP 1992-255689	19920831
PRAI	JP 1992-255689		19920831		

AB Title formation involves (1) forming a pos.(neg.)-photosensitive resist or **polyimide** column-shaped cushion bump provided on an electrode pad on a semiconductor **wafer**, (2) forming a thin-film Ti or Pd

(thickness 100-3000.ANG.) cohesive-sublayer over the pad and the cushion bump (3) forming a thin-**film** Au or **Cu** (thickness 1000.ANG.-10 .mu.m) conductor layer over the cohesive-sublayer. The coating of the bumps with the thin-**film** Au or **Cu** conductor **layer** and the thin-film Ti or Pd cohesive-sublayer gives the bump contacts thermal stress crack-proof, surface-smoothness, and decreased contact resistance properties.

IT Electric contacts
(bump, for high-frequency semiconductor devices in prevention of crack and in decrease of contact resistance)

IT Semiconductor devices
(high-frequency, formation of bump in)

IT 7440-05-3, Palladium, uses 7440-32-6, Titanium, uses
RL: DEV (Device component use); USES (Uses)
(thin-film cohesive sublayer for bump contact)

IT 7440-50-8, **Copper**, uses 7440-57-5, Gold, uses
RL: DEV (Device component use); USES (Uses)
(thin-**film elec. conductive** contact layer for bump contact)

L68 ANSWER 33 OF 46 HCAPLUS COPYRIGHT 2003 ACS
AN 1993:651807 HCAPLUS
DN 119:251807
TI **Electrically conductive** hot-press adhesive films
IN Sakamoto, Juji; Takeda, Toshiro; Takeda, Naoji
PA Sumitomo Bakelite Co, Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 05125332	A2	19930521	JP 1991-287910	19911101
PRAI	JP 1991-287910		19911101		

AB The title films, showing good adhesion after pressing for a short time at low temp. and pressure and having good heat resistance, comprise **polyimides** prepd. from acid components contg. 4,4'-oxydiphthalic dianhydride (I) and amine components contg. 1,3-bis(3-aminophenoxy)benzene (II) and **elec. conducting** fillers. A **polyimide** prepd. from 0.1 mol I and 0.1 mol II was dissolved in diglyme, mixed with powd. Ag (3 .mu.m), and cast on a Teflon surface to give a film which was pressed between a Cu lead frame and a Si **chip** at 250.degree. and 4.76 kg/cm2 for 10 s to give shear adhesion >10 kg at room temp. and 2.3 kg at 260.degree. and vol. resistivity 1 .times. 10-4 .OMEGA.-cm.

IT Semiconductor devices
(adhesive films for, **polyimide**-conducting metal powder mixts. for)

IT **Polyimides**, uses
RL: USES (Uses)
(adhesive films, hot-press, contg. **elec. conductive** powders, heat-resistant)

IT Heat-resistant materials
(adhesives, films, **polyimide-elec. conducting** powder mixts. for)

IT Adhesives
(films, heat-resistant, **polyimide-elec. conducting** powder mixts. for)

IT Siloxanes and Silicones, uses
RL: USES (Uses)

(polyether-**polyimide**-, adhesive films, hot-press, contg. **elec. conductive** powders, heat-resistant)

IT **Polyimides**, uses
RL: USES (Uses)
(polyether-siloxane-, adhesive films, hot-press, contg. **elec. conductive** powders, heat-resistant)

IT Siloxanes and Silicones, uses
RL: USES (Uses)
(**polyimide**-, adhesive films, hot-press, contg. **elec. conductive** powders, heat-resistant)

IT Polyethers, uses
RL: USES (Uses)
(**polyimide**-siloxane-, adhesive films, hot-press, contg. **elec. conductive** powders, heat-resistant)

IT **Polyimides**, uses
RL: USES (Uses)
(siloxane-, adhesive films, hot-press, contg. **elec. conductive** powders, heat-resistant)

IT 67297-90-9 72344-67-3 150773-59-4 150773-60-7 151314-44-2
RL: USES (Uses)
(adhesive films, hot-press, contg. **elec. conductive** powders, heat-resistant)

IT 7440-50-8, Copper, miscellaneous
RL: MSC (Miscellaneous)
(**polyimide** adhesive films for silicon **chips** and, hot-press, **elec. conducting**)

IT 1344-28-1, Aluminum oxide, uses 7429-90-5, Aluminum, uses 7440-02-0, Nickel, uses 7440-22-4, Silver, uses
RL: USES (Uses)
(powd., **polyimide** adhesive films contg., hot-press, **elec. conducting**)

IT 7440-21-3, Silicon, uses
RL: USES (Uses)
(**wafers**, **polyimide** adhesive **films** for **copper** and, hot-press, **elec. conducting**)

L68 ANSWER 34 OF 46 HCAPLUS COPYRIGHT 2003 ACS
AN 1993:196352 HCAPLUS
DN 118:196352
TI Manufacture of metal-coated powders with uniform thickness by mechanical alloying or mixing
IN Wada, Hitoshi; Yoshitake, Masayoshi; Kajita, Osamu
PA Fukuda Metal Foil and Powder Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 3 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 04350102	A2	19921204	JP 1991-29449	19910129
PRAI	JP 1991-29449		19910129		

AB The composite powders are manufd. by mixing of hard metal or nonmetal feed powders with foils and/or **chips** (having .ltoreq.10 .mu.m thickness) of Au, Pt, Pd, Ag, In, Ta, Ti, Zr, Mo, Co, Nb, W, Al, Ni, Fe, Cr, Cu, Sn, Pb, Zn, or their alloys, and then uniformly coating the powders by mech. mixing (esp. in ball mills). The metal-coated powders are useful for fillers for **elec. conductive** paints, magnetic materials, and electromagnetic shields.

IT Coating materials
(metals, powders with, for fillers)

IT Acrylic polymers, uses
Polyimides, uses
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(powder, manuf. of metal-coated, with uniform thickness)
IT Glass, nonoxide
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(powders, manuf. of metal-coated, with uniform thickness)
IT Electric conductors
(powders, metal coating on)
IT Glass, oxide
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(beads, manuf. of metal-coated, with uniform thickness)
IT 7429-90-5, Aluminum, uses 7439-89-6, Iron, uses 7439-92-1, Lead, uses 7439-98-7, Molybdenum, uses 7440-02-0, Nickel, uses 7440-03-1, Niobium, uses 7440-05-3, Palladium, uses 7440-06-4, Platinum, uses 7440-22-4, Silver, uses 7440-25-7, Tantalum, uses 7440-31-5, Tin, uses 7440-32-6, Titanium, uses 7440-33-7, Tungsten, uses 7440-47-3, Chromium, uses 7440-48-4, Cobalt, uses 7440-50-8, **Copper**, uses 7440-57-5, Gold, uses 7440-66-6, Zinc, uses 7440-67-7, Zirconium, uses 7440-74-6, Indium, uses
RL: USES (Uses)
(**coating**, powders manufd. with, for fillers with uniform thickness)
IT 12597-68-1, Stainless steel, uses
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(powder, manuf. of metal-coated, for fillers with uniform thickness)
IT 1314-23-4, Zirconia, uses 1344-28-1, Alumina, properties 11068-82-9, Permalloy
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(powder, manuf. of metal-coated, with uniform thickness)

L68 ANSWER 35 OF 46 HCAPLUS COPYRIGHT 2003 ACS
AN 1992:613979 HCAPLUS
DN 117:213979
TI Study of physicochemical stability of the copper/poly(phenylquinoxaline) interfaces
AU Even, R.; Palleau, J.; Oberlin, J. C.; Pantel, R.; Laviale, D.; Templier, F.; Torres, J.; Giustiniani, R.; Cros, A.
CS Lab. Chim. Electrochim. Mater. Mol., ESPCI, Paris, 75231, Fr.
SO Polyimides Other High-Temp. Polym., Proc. Eur. Tech. Symp., 2nd (1991), 407-19. Editor(s): Abadie, Marc J. M.; Sillion, Bernard. Publisher: Elsevier, Amsterdam, Neth.
CODEN: 57QVAJ
DT Conference
LA English
AB Thin film technologies were applied in building up multilayered **chip**-to-**chip** interconnections to achieve aggressive requirements such as high elec. performance or extreme compactness. Cu as conductor and a new **polymeric** material, poly(phenylquinoxaline) (I), as dielec. were chosen to fulfill demanding elec. and phys. conditions. Thermal stability at the I-Cu interface during the curing process was very important to preserve good adhesion between the conductor and dielec. materials. The interfacial behavior was studied as a function of annealing temp. and of annealing atm. In the case of Cu presence, the O pollution, even at low level, was detrimental for polymer integrity. Exptl. results gave a clear indication of catalytic degrdn. of the polymer in presence of Cu oxide. A thin Cr layer intervening between the **Cu** and I **films** was a very efficient O diffusion barrier blocking any Cu oxide formation and hence any enhanced polymer degrdn.
IT Electric conductors
(copper, interfaces with poly(phenylquinoxaline) insulators,

physicochem. stability of)
IT Interface
(copper-poly(phenylquinoxaline), physicochem. stability of)
IT Polyquinoxalines
RL: USES (Uses)
(interfaces with copper, physicochem. stability of)
IT Electric insulators and Dielectrics
(poly(phenylquinoxaline), interfaces with copper conductors, physicochem. stability of)
IT 63713-51-9
RL: USES (Uses)
(interfaces with copper, physicochem. stability of)
IT 7440-50-8, Copper, properties
RL: PRP (Properties)
(interfaces with poly(phenylquinoxaline), physicochem. stability of)

L68 ANSWER 36 OF 46 HCAPLUS COPYRIGHT 2003 ACS
AN 1992:164124 HCAPLUS
DN 116:164124
TI Packaging technology for IBM's latest mainframe computers (S/390/ES9000)
AU Tummala, R. R.; Potts, H. R.; Ahmed, Shakil
CS IBM Corp., East Fishkill, NY, USA
SO Proceedings - Electronic Components & Technology Conference (1991), 41st., 682-8
CODEN: PETCES
DT Journal
LA English
AB The IBM system 390/ES9000 mainframe computers, models 820 and 900, are significantly enhanced by a revolutionary set of packaging materials. These new materials, glass ceramic and copper conductors, were developed over the last decade and integrated into the pioneering thermal conduction module introduced by IBM in 1980. The new substrate is based on the crystn. of an unique glass to form a glass-ceramic having a dielec. const. of 5.2 relative to 9.4 with the previous alumina material. The copper conductor exhibits a 3-fold improvement in **elec. cond.** over molybdenum. A novel sintering process, developed for the glass-ceramic substrate, provides the industry's best dimensional control that results in the closest placement of metal vias to date. Each substrate with 63 metal layers measures 127.5 mm square and can support up 121 complex logic and memory array **chips.** The base glass-ceramic substrate is further enhanced by **polyimide-copper** thin **film** redistribution.
IT Sintering
(in packaging of mainframe computers)
IT Computers
(mainframe, packaging technol. for)
IT Glass ceramics
(substrates, in packaging of mainframe computers)
IT Electronic device packaging
(with copper and glass ceramic of mainframe computers)
IT 7440-21-3, Silicon, uses
RL: USES (Uses)
(computer based on, packaging in fabrication of, copper and glass ceramic for)
IT 1344-28-1, Aluminum sesquioxide, uses 7439-98-7, Molybdenum, uses 7440-50-8, Copper, uses
RL: USES (Uses)
(in packaging of mainframe computers)

L68 ANSWER 37 OF 46 HCAPLUS COPYRIGHT 2003 ACS
AN 1991:657820 HCAPLUS

DN 115:257820
TI Self-fusible electrical insulators and coils
IN Kamioka, Isao
PA Sumitomo Electric Industries, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 03089414	A2	19910415	JP 1989-227784	19890901
PRAI	JP 1989-227784		19890901		

AB The title insulators with good heat distortion prevention comprise **elec. conductors**, insulating layers, and self-fusible layers (A) consisting of arom. polyamides with glass-transition temp. (Ig) .gtoreq.90.degree. and 5-40% (based on A) polyamides (m.p. 50-150.degree.) as the outer layers. Thus, a **copper** coil **coated** with 0.020-mm Isomid RH (polyester-imide) then with 0.008-mm Ultramid **IC**-Grilamid TR 55 blend (Ig 105.degree.), and with 0.002-mm T 450 (polyamide, m.p. 110.degree.) showed distortion 0.50 mm initially and 0.60 mm after 1 day at 80.degree..

IT Electric insulators and Dielectrics
(self-fusible, multilayer, consecutively with polyamide-arom. polyamide-polyester imide, for heat distortion resistance)

IT Polyamides, uses and miscellaneous
RL: USES (Uses)
(arom., self-fusible elec. insulators from, for heat distortion resistance)

IT **Polyimides**, uses and miscellaneous
RL: USES (Uses)
(polyester-, insulating layers, polyamide-arom. polyamide on, for heat distortion-resistant elec. coils)

IT Polyesters, uses and miscellaneous
RL: USES (Uses)
(**polyimide**-, insulating layers, polyamide-arom. polyamide on, for heat distortion-resistant elec. coils)

IT 25053-13-8
RL: USES (Uses)
(arom. polyamide blends, self-fusible elec. insulators from, heat-distortion-resistant)

IT 137397-71-8, Isomid RH
RL: USES (Uses)
(insulating layers, polyamide-arom. polyamide on, for heat distortion-resistant elec. coils)

IT 24937-16-4, T 450 79331-75-2 137463-82-2, Daiamid T 250
RL: USES (Uses)
(self-fusible elec. insulators from, for heat distortion resistance)

L68 ANSWER 38 OF 46 HCAPLUS COPYRIGHT 2003 ACS
AN 1990:425220 HCAPLUS
DN 113:25220
TI Epoxy adhesives for bonding insulating polymer films to metal layers in hydrid **integrated circuit** manufacture
IN Okawa, Koji; Yoshioka, Michihiko
PA Mitsubishi Cable Industries, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 01276789	A2	19891107	JP 1988-105804	19880428
PRAI	JP 1988-105804		19880428		

AB Adhesives for bonding intermediate **polyimide** insulating films to metal bases and circuit-forming **elec. conducting** metallic foils comprise 30-80 parts reaction products of a novolak epoxy resin with a bisphenol A-based epoxy resin (I) having epoxy equiv (E) 180-200, 70-20 parts I with E 900-2100, crosslinking agents, and accelerators. Thus, a 60% MEK soln. of ZX-661 (epoxy resin, E 482 g/equiv) and a 50% soln. of I (E 949 g/equiv) in 1:1 Me Cellosolve/MEK were mixed with 10% soln. of dicyandiamide in 1:1 Me Cellosolve/DMF and 1% 2-ethyl-4-methylimidazole in MEK in a solids ratio 70:30:1.5:0.2 to give an adhesive. An assembly of 35-.mu.m Cu foil, 25-.mu.m **polyimide** film, and 3.0-mm Al base bonded by the adhesive (13 .mu.m-thick) was press-cured 60 min at 180.degree. to give a laminate with peel strength in the **Cu**/adhesive **layers** 2.3 and 2.5 kg/cm initially and after the solder-bath heat test resp., and good resistance to solder-bath heat test and pressure-cooker test, vs. 2.1, 0.1, and poor, resp., in absence of the I.

IT Epoxy resins, uses and miscellaneous
RL: TEM (Technical or engineered material use); USES (Uses)
(adhesives, for bonding of **polyimide** insulator film in hybrid **integrated circuit** manuf.)

IT **Polyimides**, uses and miscellaneous
RL: USES (Uses)
(insulator films, adhesives for bonding of, epoxy resin-based, in hybrid **integrated circuit** manuf.)

IT Electric insulators and Dielectrics
(**polyimide** films, adhesives for bonding of, epoxy resin-based, in hybrid **integrated circuit** manuf.)

IT Heat-resistant materials
(adhesives, moisture-resistant, epoxy resin-based, for bonding **polyimide** insulator films in hybrid **integrated circuit** manuf.)

IT Adhesives
(heat- and moisture-resistant, epoxy resin-based, for bonding **polyimide** insulator films in hybrid **integrated circuit** manuf.)

IT Electric circuits
(hybrid integrated, adhesives for manuf. of, epoxy resin-based, with improved heat and moisture resistance)

IT 127778-34-1P
RL: TEM (Technical or engineered material use); PREP (Preparation); USES (Uses)
(adhesives, manuf. of, for bonding **polyimide** insulator films in hybrid **integrated circuit** manuf.)

IT 7429-90-5, Aluminum, uses and miscellaneous
RL: USES (Uses)
(base sheets, adhesive for bonding of, epoxy resin-based, in hybrid **integrated circuit** manuf.)

IT 7440-50-8, Copper, uses and miscellaneous
RL: USES (Uses)
(foil, adhesive for bonding of, epoxy-resin-based, in hybrid **integrated circuit** manuf.)

IT 120478-32-2, Kapton 200XT 127496-30-4, Upilex 25R
RL: USES (Uses)
(insulator films, adhesive for bonding of, epoxy resin-based, in hybrid **integrated circuit** manuf.)

L68 ANSWER 39 OF 46 HCAPLUS COPYRIGHT 2003 ACS

AN 1989:449064 HCAPLUS
DN 111:49064
TI Metal-core board for hybrid **integrated circuits** and method for manufacturing it
IN Shirai, Hideaki; Chibia, Kimio; Okawa, Koji; Ishibashi, Hiroshi; Ishii, Akihiro; Itoh, Hirotaka; Kuzushita, Hirokazu; Yoshioka, Michihiko; Hirose, Michio
PA Dainichi Nippon Cables, Ltd., Japan
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 3

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 4695515	A	19870922	US 1985-759210	19850726
	JP 61148899	A2	19860707	JP 1984-271425	19841222
	JP 04021358	B4	19920409	JP 1984-271426	19841222
PRAI	JP 1984-U118195		19840730		
	JP 1984-U118196		19840730		
	JP 1984-271425		19841222		
	JP 1984-271426		19841222		

AB The board has a base metal core, a layer of an easily solderable metal formed by plating on both sides of the core, an elec. insulating layer on 1 easily solderable metal layer, and an **elec. conductive** metal layer on the insulating layer. An Al plate 1-mm thick was treated with NaOH soln. to remove Al oxide from the surface, coated with Zn by electroless plating, and then with Cu by electroplating. One of the **Cu layers** was masked by PVC visco-adhesive tape, and the other was roughened and coated electrophoretically with epoxy-acrylic varnish. The varnish was treated with DMF and cured at 150.degree. for 30 min. A Cu foil was then adhered to the varnish, using an adhesive, by pressing at 20 kg/cm2 and 200.degree.. A board .apprx.1.1-mm thick was obtained.

IT **Polyimides**, uses and miscellaneous
RL: TEM (Technical or engineered material use); USES (Uses)
(elec. insulators, in metal-core boards for hybrid **integrated circuits**)

IT Solders
(metal cores plated with, for boards for hybrid **integrated circuits**)

IT Electric insulators and Dielectrics
(metal-core boards contg., for hybrid **integrated circuits**)

IT Epoxy resins, uses and miscellaneous
RL: TEM (Technical or engineered material use); USES (Uses)
(acrylic, elec. insulators, in metal-core boards for hybrid **integrated circuits**)

IT Acrylic polymers, uses and miscellaneous
RL: TEM (Technical or engineered material use); USES (Uses)
(epoxy, elec. insulators, in metal-core boards for hybrid **integrated circuits**)

IT Electric circuits
(hybrid integrated, boards, metal-core, having easily solderable metal and elec. insulator layers)

IT Glass fibers, uses and miscellaneous
RL: USES (Uses)
(textiles, elec. insulators from epoxy resins reinforced with, in boards for hybrid **integrated circuits**)

IT Aluminum alloy, base
Iron alloy, base

RL: USES (Uses)
(boards having cores of, for hybrid **integrated circuits**)

IT 7429-90-5, Aluminum, uses and miscellaneous 7439-89-6, Iron, uses and miscellaneous 12597-69-2, Steel, uses and miscellaneous
RL: USES (Uses)
(boards having cores of, for hybrid **integrated circuits**)

IT 25852-42-0, Acrylic acid-ethyl acrylate-methylol acrylamide copolymer 35705-87-4, Acrylic acid-acrylonitrile-glycidyl methacrylate-styrene copolymer 57604-74-7, Acrylic acid-acrylonitrile-glycidyl methacrylate copolymer 57604-75-8 57604-76-9, Acrylonitrile-glycidyl methacrylate-maleic acid copolymer
RL: USES (Uses)
(elec. insulating varnish, in metal-core boards for hybrid **integrated circuits**)

IT 40364-42-9
RL: USES (Uses)
(elec. insulators from glass cloth impregnated with, in metal-core boards for hybrid **integrated circuits**)

IT 106043-65-6, V 551-20
RL: TEM (Technical or engineered material use); USES (Uses)
(elec. insulators, in metal-core boards for hybrid **integrated circuits**)

IT 7439-92-1, Lead, uses and miscellaneous 7440-02-0, Nickel, uses and miscellaneous 7440-22-4, Silver, uses and miscellaneous 7440-31-5, Tin, uses and miscellaneous 7440-50-8, Copper, uses and miscellaneous 7440-57-5, Gold, uses and miscellaneous
RL: USES (Uses)
(metal cores plated with, for boards for hybrid **integrated circuits**)

L68 ANSWER 40 OF 46 HCAPLUS COPYRIGHT 2003 ACS
AN 1989:164446 HCAPLUS
DN 110:164446
TI Preparation of **electrically conductive** bridges for hybrid **integrated circuits**
IN Uchida, Katsutoshi; Arai, Kazuya
PA Sanyo Electric Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 3 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 63261779	A2	19881028	JP 1987-95564	19870417
PRAI	JP 1987-95564		19870417		

AB The title process involves: (a) attaching a **metal** (e.g., **Cu**) foil-covered insulator (e.g., **polyimide**) film to a pair of mutually sepd. metal (e.g., Al) substrates; (b) placing a support (e.g., from Al) on the exposed side of the substrates, where the support has a mesa fitting into the recess between the 2 substrates; (c) press-attaching a photoresist film to the metal foil with the use of a roller; (d) patterning the resist film into a predetd. configuration; and (e) etching the exposed part of the metal foil with the resist film as a mask. The metal foil bridging the 2 substrates is not likely to break due to bending.

IT Electric conductors
(bridges, for hybrid **integrated circuits**, prepn. of)

IT **Polyimides**, uses and miscellaneous
RL: PREP (Preparation)
(hybrid **integrated circuits** contg., prepn. of copper bridges for)
IT 7440-50-8, Copper, uses and miscellaneous
RL: USES (Uses)
(bridges from, for hybrid **integrated circuits**, prepn. of)
IT 7429-90-5, Aluminum, uses and miscellaneous
RL: USES (Uses)
(hybrid **integrated circuits** with substrates of, prepn. of copper bridges for)

L68 ANSWER 41 OF 46 HCAPLUS COPYRIGHT 2003 ACS
AN 1988:497453 HCAPLUS
DN 109:97453
TI Method for increasing retention of solderability of metal conductors
IN Mehan, Ashok K.; Lunk, Hans E.
PA Raychem Corp., USA
SO Eur. Pat. Appl., 6 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 270210	A2	19880608	EP 1987-308006	19870910
	EP 270210	A3	19881102		
	EP 270210	B1	19920708		
	R: AT, BE, CH, DE, ES, FR, GB, IT, LI, NL, SE				
	US 4876116	A	19891024	US 1986-906355	19860911
	AT 78065	E	19920715	AT 1987-308006	19870910
PRAI	US 1986-906355		19860911		
	EP 1987-308006		19870910		

AB The retention of solderability of conductors (Cu, **Cu** alloy, Sn-**coated Cu** stranded wire, Cu- or **Cu** alloy-**coated** steel core) exposed to humid environments or steam aging is increased by coating or treating them with a surface-active agent with an HLB value <10. The conductors are part of a printed wire assembly, a lead on an elec. component, or a contact pad on a leadless **chip** component, which is suitable for connection by soldering to another **elec. conductor**. For a conductor with an insulating **polymeric** jacket, the **polymeric** insulating compn. is formed on the conductor surface carrying the surface-active agent. Thus, a stranded Sn-plated Cu wire (outside diam. 0.08 cm) was dipped into baths contg. either a halogenated solvent (Freon 113) or a mineral oil-25% petroleum solvent and 5% surfactant (span 85). The resp. solder coverage in MS 202F-208 test after steam aging for 8, 16, and 24 h for the surface-treated wire were 99, 97, and 88% vs. 87, 53, and 52% for an untreated wire.
IT Electric conductors
(tin-**coated copper**, solderability retention in humid atm. of, treatment with surfactant for)
IT 110-25-8, Oleoylsarcosine 1338-39-2, Emsorb 2515 1338-43-8, Emsorb 2500 9005-65-6, Tween 80 9016-45-9, Polyethylene glycol nonylphenyl ether 26266-58-0, Emsorb 2503 27253-29-8, Zinc neodecanoate
RL: USES (Uses)
(surfactant, for treatment of **elec. conductor** for solderability retention in humid atm.)
IT 7440-50-8, **Copper**, properties
RL: PRP (Properties)

(tin-**coated**, stranded wire of, solderability retention in humid atm. of, surfactant treatment for)

L68 ANSWER 42 OF 46 HCAPLUS COPYRIGHT 2003 ACS
AN 1987:588938 HCAPLUS
DN 107:188938
TI Semiconductor packaging featuring copper/**polyimide** multilayer tape
AU Ballard, William V.; Cardashian, Vahram S.
CS 3M Co., USA
SO Proceedings - Electronic Components Conference (1986), 36th, 556-9
CODEN: PECCA7; ISSN: 0569-5503
DT Journal
LA English
AB A high-d. interconnect system which facilitates multiple-**die** mounting is described which uses a Cu/**polyimide** substrate with 2 conductor layers for **chip** mounting. The fabrication of this multilayer tape and its performance evaluation are described.
IT **Polyimides**, uses and miscellaneous
RL: USES (Uses)
(adhesive tape from copper and, for semiconductor packaging)
IT Adhesive tapes
(copper-**polyimide**, for semiconductor packaging)
IT Lithography
(in copper-**polyimide** tape prepn. for semiconductor-device fabrication)
IT Semiconductor devices
(packaging of, with copper-**polyimide** adhesive tape)
IT 7429-90-5, Aluminum, uses and miscellaneous
RL: USES (Uses)
(bonding of wires of, to copper tape for semiconductor packaging)
IT 7440-02-0, Nickel, uses and miscellaneous 7440-31-5, Tin, uses and miscellaneous 7440-57-5, Gold, uses and miscellaneous
RL: USES (Uses)
(**elec. conductor coating** of, on **copper** for multilayer tape for semiconductor packaging)
IT 7440-50-8, Copper, uses and miscellaneous
RL: USES (Uses)
(multilayer **polyimide** adhesive tape from, for semiconductor packaging)

L68 ANSWER 43 OF 46 HCAPLUS COPYRIGHT 2003 ACS
AN 1986:27212 HCAPLUS
DN 104:27212
TI Fine-line, multilayer hybrids with wet-processed conductors and thick-film resistors
AU Takasago, Hayato; Takada, Mitsuyuki; Adachi, Kohei; Endo, Atsushi; Yamada, Kurumi; Onishi, Yoichiro; Morihiro, Yoshiyuki
CS Mater. Eng. Lab., Mitsubishi Electr. Corp., Amagasaki, 661, Japan
SO Proceedings - Electronic Components Conference (1984), 34th, 324-9
CODEN: PECCA7; ISSN: 0569-5503
DT Journal
LA English
AB Title hybrid circuits were obtained from a material combination of wet-**metalized Cu**, air-fired RuO2 resistor paste, and photoactive **polyimide**. The hybrids were constructed on alumina substrates and the **chip** components were reflow-soldered. Both the top and bottom conductors had ample adherence and heat-resistance-related features were excellent. Materials and process design concepts and reliability evaluations are discussed in detail.
IT Electric circuits

(multilayer, hybrid fine-line, fabrication and reliability of)
IT Electric resistors
(thick-film, ruthenium oxide, in fine-line multilayer hybrid circuits)
IT 7440-50-8, uses and miscellaneous
RL: USES (Uses)
(**elec. conductors** from wet-processed, in fine-line multilayer hybrid circuits)

L68 ANSWER 44 OF 46 HCAPLUS COPYRIGHT 2003 ACS
AN 1975:507127 HCAPLUS
DN 83:107127
TI Formation of corrosion resistant electronic interconnections
IN Cook, Herbert Carl; Farrar, Paul A.; Hallen, Robert L.
PA International Business Machines Corp., USA
SO U.S., 6 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 3881884	A	19750506	US 1973-406125	19731012
	DE 2440481	A1	19750424	DE 1974-2440481	19740823
	FR 2247820	A1	19750509	FR 1974-30003	19740830
	GB 1448034	A	19760902	GB 1974-40376	19740917
	JP 50068082	A2	19750607	JP 1974-107848	19740920
	SE 7412333	A	19750414	SE 1974-12333	19741001
	SE 401291	B	19780424		
	SE 401291	C	19780803		
	CH 569363	A	19751114	CH 1974-13188	19741001
	NL 7413310	A	19750415	NL 1974-13310	19741009
	BR 7408490	A0	19750729	BR 1974-8490	19741011
PRAI	US 1973-406125		19731012		

AB A method is described for the manuf. of composite thin films useful as electronic **microcircuit** interconnections, fuses, and contacts. The method consists of carrying out an **integrated circuit** fabrication process consisting of first depositing a barrier layer of antidiffusion material such as Cr, followed by superimposing thereon a film of highly conductive metals susceptible to corrosion (i.e., Cu) and followed by the deposition of a highly corrosive resistant metal film (i.e., Au). A subtractive etch pattern is formed in the composite metal film, and then the structure is heated to an elevated temp. for a predetd. time so that the uppermost layer of the composite flows by diffusion over the edge section to protect the conductive metal film from corrosive effects. Heat treatment conditions are specified for the cases involving quartz or **polyimide** substrates. When the substrate is covered with quartz, the Cr-Cu-Au composite is heated in H2 at 345-355.degree..
IT Electric circuits
(integrated, corrosion-resistant metalization for, heat-treated chromium-**copper**-gold composite **film** structures for)
IT Electric conductors
(metalization, heat-treated chromium-**copper**-gold composite **film** structures for corrosion-resistant, in **integrated circuits**)
IT 7440-47-3, uses and miscellaneous 7440-50-8, uses and miscellaneous
7440-57-5, uses and miscellaneous
RL: USES (Uses)
(**elec. conductive metalization** from chromium-**copper**-gold composite **film** structures, heat-treated for corrosion resistance)

L68 ANSWER 45 OF 46 HCAPLUS COPYRIGHT 2003 ACS
AN 1973:457078 HCAPLUS
DN 79:57078
TI Depositing metallic patterns on electrically nonconductive substrates
IN Lando, David Jacob
PA Western Electric Co., Inc.
SO Ger. Offen., 42 pp.
CODEN: GWXXBX
DT Patent
LA German
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	DE 2256960	A1	19730530	DE 1972-2256960	19721121
	DE 2256960	B2	19760715		
	DE 2256960	C3	19770310		
	US 3793072	A	19740219	US 1971-202305	19711126
	CA 998577	A1	19761019	CA 1972-144449	19720612
	BE 791374	A1	19730301	BE 1972-124150	19721114
	HU 165278	P	19740727	HU 1972-WE474	19721120
	AU 7249105	A1	19740523	AU 1972-49105	19721121
	GB 1413810	A	19751112	GB 1972-53925	19721122
	NL 7215981	A	19730529	NL 1972-15981	19721124
	FR 2161101	A1	19730706	FR 1972-41955	19721124
	IT 975851	A	19740810	IT 1972-70704	19721124
	ES 409263	A1	19751001	ES 1972-409263	19721125
	JP 48060026	A2	19730823	JP 1972-118119	19721127
	US 3873358	A	19750325	US 1973-388841	19730816
	US 3873360	A	19750325	US 1973-388844	19730816
	US 3873357	A	19750325	US 1973-388866	19730816
	US 3873359	A	19750325	US 1973-388843	19730816
	US 3900614	A	19750819	US 1973-388842	19730816
	CA 999193	A2	19761102	CA 1976-244057	19760122
PRAI	US 1971-202305		19711126		
	CA 1972-144449		19720612		

AB Adherent, **elec. conductive** metal **coatings**, such as **Cu**, are electrolessly deposited on dielec. substrates after conditioning by selective sensitizing, imprinting, and activation. The metal-coated composite is used for elec. switches or circuits. Sensitivity to the dielec. surface is imparted by coating it with a stable, colloidal suspension of basic oxides of Ti, V, Cr, Fe, Sn or Pb, at a pH which prevents flocculation of the suspended particles. The desired pattern is imprinted on the surface by a **die**, e.g. a rubber stamp. The raised portions of the **die** are coated with an oxidizer, such as MnO42-, which when in contact with the colloidal suspension causes oxidn. of the colloidal suspension at selected locations. These oxidized surfaces are then activated by immersion in a Pd2+ or Pt2+ soln. Subsequently, the activated surface is electrolessly coated with a conductive metal. Thus, the surface of a **polyimide** substrate was sensitized with a colloidal suspension of the basic Sn oxide. A rubber stamp was then immersed in a 1 wt. % KMnO4 contg. H2SO4, and then applied to the sensitized surface. The treated substrate was then immersed in an 0.05 wt. % PdCl2, followed by rinsing and electroless coating with an 8 .times. 10-5 cm thick **Cu layer**. A strong, adherent **Cu coating** was obtained in the desired pattern.

IT Electric circuits
(stamping process for activation of areas for copper deposition on)

IT **Coating** process
(with **copper**, on printed surfaces with stamped activation

areas)
IT 7440-50-8, uses and miscellaneous
RL: USES (Uses)
(coating with, on printed circuits by stamping activation of surface)

L68 ANSWER 46 OF 46 HCAPLUS COPYRIGHT 2003 ACS
AN 1967:491771 HCAPLUS
DN 67:91771
TI Insulating coatings for **electrical conductors**
IN Rating, Wilhelm; Von Bornhaupt, Bernd
PA Firma Dr. Kurt Herberts and Co.; /Firma Dr. Kurt Herberts and Co.
SO Ger. (East), 8 pp.
CODEN: GEXXA8
DT Patent
LA German
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI DD 55363		19670420		
PRAI DE		19650601		

AB Insulatihg coatings with improved thermostability are prepd. from ester amide imido condensation products. The condensation products may contain end groups of polybasic carboxylic acids, polyhydric alcs., as well as polyhydric phenols, and amino groups capable of amide or ester formation as well as five membered imide rings. Thus, a mixt. of trimellitic anhydride (I) 2.6, 4,4'-diaminodiphenyl-methane (II) 2.0, and ethylene glycol (III) 7.0 moles was treated with 0.005 mole Zn(OAc)2. The addn. of I and II to III followed in 6 equal portions. The H2O was distd. after each addn. The first addn. took place at 120.degree. and during the process of the reaction the temp. was raised to 220.degree.. After the removal of 5.2 moles H2O, 3.2 moles excess III was distd. without the use of a column. The clear, reddish brown, very viscous melt had reached a temp. of 250.degree. at this stage. The resin viscosity was 2955 cp., measured in a 33% m-cresol (IV) soln. at 25.degree.. After diln. of the melt with crude cresol to 75% solid content at 180.degree., 6 g. **polymeric** Bu titanate was added and evenly dispersed in the resin soln. A mixt. was dild. with crude IV to 50% solid content, and 56 parts removed to which were added addnl. crude IV 20, solvent naphtha 10, Tetralin 8, xylene 4, and propylene glycol 2 parts. The wire lacquer thus obtained had a pour consistency of 85 sec. (4 mm. **die**, 20.degree.) and a solid content of 20%. A Cu wire of 0.9 mm. diam. was coated with 8 layers in a wire coating oven of 2.7 m. length at 450.degree. at a rate of 6 m./min. The lacquer-coated wire had the following properties: thickness of lacquer 28 .mu.m., pencil hardness 2 H, scrape resistance 37, adhesion 400, dielec. strength 150 v./.mu. m., char resistance 16 min., and thermoplasticity at 200.degree. 82%, at 250.degree. 32%, and at 300.degree. 17%.

L75 ANSWER 1 OF 47 HCAPLUS COPYRIGHT 2003 ACS
AN 2003:286843 HCAPLUS
TI Filter optimization for X-ray inspection of surface-mounted **ICs**
AU Blish, Richard C., II; Li, Susan X.; Lehtonen, David
CS Advanced Micro Devices, Sunnyvale, CA, 94088, USA
SO IEEE Transactions on Device and Materials Reliability (2002), 2(4), 102-106
CODEN: ITDMA2; ISSN: 1530-4388
URL: http://ieeexplore.ieee.org/xpl/tocresult.jsp?isNumber=26408
PB Institute of Electrical and Electronics Engineers
DT Journal; (online computer file)
LA English
AB A thin Zn filter (.apprx. 300 .mu.m) and relatively low X-ray tube voltage (.apprx. 45 kV) is recommended for X-ray inspection of surface-mounted device solder joints on printed wiring boards (PWBs). An optimal filter minimizes the Si dose that could result in cumulative damage to sensitive **integrated circuit** (**IC**) nodes, yet provides good contrast for **metals** such as **Cu** traces on PWBs and device **solder balls**. While we expect orders of magnitude Si dose redns. when effective filters are inserted, a properly chosen filter should not attenuate the portion of the white X-ray spectrum required to image Cu, **Sn**, and **Pb** (**solder balls**). Some X-ray inspection suppliers can achieve a Si dose of as little as 0.060 rads, while other X-ray inspection suppliers, not yet optimized for min. dose, may use as much as four orders of magnitude more dose. We used thermo luminescent detectors (TLDs) to measure the X-ray dose that **IC** product shipments would encounter during a shipping process, for example, as personal baggage or cargo, as .ltoreq. 0.050 rads.
RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L75 ANSWER 2 OF 47 HCAPLUS COPYRIGHT 2003 ACS
AN 2003:283668 HCAPLUS
TI Interface reactions and phase equilibrium between Ni/**Cu** under-bump **metallization** and eutectic SnPb flip-**chip** **solder bumps**
AU Huang, Chien-Sheng; Duh, Jenq-Gong
CS Department of Materials Science and Engineering, National Tsing Hua University, Hsinchu, Taiwan
SO Journal of Materials Research (2003), 18(4), 935-940
CODEN: JMREEE; ISSN: 0884-2914
PB Materials Research Society
DT Journal
LA English
AB Ni-based under-bump metalization (UBM) for flip-**chip** application is widely used in today's electronics packaging. In this study, electroplated Ni UBM with different thickness was used to evaluate the interfacial reaction during multiple reflow between Ni/Cu UBM and eutectic **Sn-Pb** solders in the 63Sn-37Pb/Ni/Cu/Ti/Si3N4/Si multilayer structure. During the first cycle of reflow, Cu atoms diffused through electroplated Ni and formed the intermetallic compd. (IMC) (Ni1-x,Cux)3Sn4. After more than three times of reflow, Cu atoms further diffused through the boundaries of (Ni1-x,Cux)3Sn4 IMC and reacted with Ni and **Sn** to form another IMC of (Cu1-y,Niy)6Sn5. After detailed quant. anal. by electron probe microanal., the values of y were evaluated to remain around 0.4; however, the values of x varied from 0.02 to 0.35. The elemental distribution of IMC in the interface of the joint assembly could be correlated to the Ni-Cu-**Sn** ternary equil. In addn., the mechanism of (Cu1-y,Niy)6Sn5 formation was also probed.

RE.CNT 18 THERE ARE 18 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L75 ANSWER 3 OF 47 HCAPLUS COPYRIGHT 2003 ACS
AN 2003:77496 HCAPLUS
DN 138:129917
TI Deposition of electroplate solder beads on electric-circuit board for flip-**chip** soldering joints
IN Hsieh, Han-Kun; Wang, Shing-Ru; Tung, I-Chung
PA Taiwan
SO U.S. Pat. Appl. Publ., 16 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 2

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2003022477	A1	20030130	US 2001-52989	20011109
TW 2001-90118363	A	20010727		

PI
PRAI

AB A method of fabricating electroplate solder on an org. circuit board for forming flip **chip** joints and board to board solder joints is disclosed. In the method, there is initially provided an org. circuit board including a surface bearing elec. circuitry that includes at least one contact pad. A solder mask layer that is placed on the board surface and patterned to expose the pad. Subsequently, a metal seed layer is deposited by phys. vapor deposition, chem. vapor deposition, electroless plating with the use of catalytic copper, Ni, Cr, Ti, Cu-Cr alloy, or **Sn-Pb**, or electroplating with the use of catalytic copper, over the board surface. A resist layer with at least an opening located at the pad is formed over the metal seed layer. A solder is then formed in the opening by electroplating. The solder contains .gtoreq.1 **Sn**, **Pb**, Ag, Cu, Bi, Sb, Zn, Al, Ni, In, Mg, Ga, and Te. Finally, the resist and the metal seed layer beneath the resist are removed.

L75 ANSWER 4 OF 47 HCAPLUS COPYRIGHT 2003 ACS
AN 2003:67821 HCAPLUS
DN 138:224902
TI Reaction kinetics of **Pb-Sn** and **Sn-Ag** **solder balls** with electroless Ni-P/**Cu** **pad** during reflow soldering in **microelectronic** packaging
AU Alam, M. O.; Chan, Y. C.; Hung, K. C.
CS Department of Electronic Engineering, City University of Hong Kong, Kowloon Tong, Hong Kong
SO Proceedings - Electronic Components & Technology Conference (2002), 52nd, 1650-1657
CODEN: PETCES
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
AB Detailed microstructural studies were carried out to compare the reaction kinetics of **Pb-Sn** solder and **Sn-Ag** solder with electroless Ni-P layer for different reflow times. **Sn-Ag** solder reacts at a faster rate with electroless Ni-P layer to form Ni-**Sn** intermetallic compd. (IMC) and hence P-rich layer is formed quickly by expellation of the P from the reacting Ni-P layer. Ni-**Sn** reaction at the interface of molten **Sn-Ag** solder with electroless Ni-P is so much quicker, resulting in the entrapment of some P in the Ni-**Sn** IMC. The initial P content in the electroless Ni-P layer is around 20 at.%. However, as high as 38 at.% P is detected in the dark Ni-P layer at the **Sn-**

Ag solder interface. After 180 min reflow of the **Sn-Ag** solder joint, the Ni-P layer is found to disappear, leading to the full conversion of the 15 .mu.m **Cu pad** to **Cu-Sn** IMC. On the contrary, Ni-**Sn** IMC growth rate in **Pb-Sn** solder interface is slower as well as more adherent. For 180 min reflow of the **Pb-Sn** solder interface, the electroless Ni-P layer is found to act as a diffusion barrier for **Sn** towards **Cu pad**. Its implications for leadfree soldering will be highlighted.
RE.CNT 30 THERE ARE 30 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L75 ANSWER 5 OF 47 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:978551 HCAPLUS
DN 138:47095
TI Interconnect structure and process for silicon optical bench
IN Ray, Sudipta K.; Cohen, Mitchell S.; Herron, Lester Wynn; Interrante, Mario J.; Lombardi, Thomas E.; Shinde, Subhash L.
PA International Business Machines Corporation, USA
SO U.S. Pat. Appl. Publ., 10 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 2002196996	A1	20021226	US 2001-885791	20010620
PRAI US 2001-885791		20010620		

AB A method of fabricating an optical subassembly in an **integrated circuit** is described entailing defining elec. conducting lines and bonding pads in a **metalization** layer (Cr/**Cu**/Ni/Au/Cr layers) on a substrate; depositing a passivation layer over the metalization layer; etching the passivation layer to remove the passivation layer from each of the bonding pads and a portion of the metalization layer assocd. with each of the bonding pads; diffusing Cr from the lines proximate the bonding pads to prevent solder wetting down lines; bonding an optical device to one of the bonding pads; and attaching the substrate to a carrier utilizing solder bond attachment. An optical subassembly in an **integrated circuit** is also described comprising a carrier having a first side and a second side; a **ball grid** array depending from the second side; a cavity disposed in the first side, a silicon optical bench (SiOB) having an optical device mounted thereon, the SiOB is elec. and mech. connected to the first side utilizing surface mount technol. attachment, the cavity providing clearance for the optical device when connecting the SiOB to the carrier, the SiOB having a metalization layer providing both wire bondable and solder bondable pads.

L75 ANSWER 6 OF 47 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:859089 HCAPLUS
DN 138:129725
TI Influence of substrate metallization on diffusion and reaction at the under-bump metallization/solder interface in flip-**chip** packages
AU Zhang, F.; Li, M.; Chum, C. C.; Tu, K. N.
CS Institute of Materials Research and Engineering (IMRE), Singapore, 117602, Singapore
SO Journal of Materials Research (2002), 17(11), 2757-2760
CODEN: JMREEE; ISSN: 0884-2914
PB Materials Research Society
DT Journal
LA English

AB In flip-**chip** packages, the effect of Ni metalization on the substrate side on interfacial reactions between solders and an Al/Ni(V)/**Cu** under-bump **metalization** (UBM) on the **chip** side was studied during the reflow process. The Ni substrate metalization greatly accelerated interfacial reactions on the **chip** side and quickly degraded the thermal stability of the UBM due to a fast consumption of the Ni(V) layer. This phenomenon can be explained in terms of rapid Ni or **Sn** diffusion in the ternary (Cu,Ni)6Sn5 phase, which was formed in the solder adjacent to the Ni(V) layer and the enhanced dissoln. of (Cu,Ni)6Sn5 into the molten solder. Without the Ni metalization on the substrate side, the Al/Ni(V)/Cu UBM remained very stable with both eutectic SnPb and **Pb**-free solders.

RE.CNT 16 THERE ARE 16 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L75 ANSWER 7 OF 47 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:660106 HCAPLUS
DN 137:328032
TI Growth prediction of **tin**/copper intermetallics formed between 63/37 **Sn**/**Pb** and OSP coated **copper** solder **pads** for a flip **chip** application
AU Grilletto, Carlo; Arroyave, Carlos M.; Govind, Anand; Salvaleon, Efren R.
CS LSI Logic Corporation, Milpitas, CA, 95035, USA
SO IEEE Transactions on Electronics Packaging Manufacturing (2002), 25(2), 78-83
CODEN: ITEPFL; ISSN: 1521-334X
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
AB This study quantifies the effect of temp. and time on the growth of Cu-**Sn** intermetallics, specifically for flip **chip**/**ball grid** array (**BGA**) packaging technol. The activation energy and the growth rates were detd. for solid state diffusion, after the initial assembly reflow(s). Three different types of solder joints were investigated. (1) **BGA** 63/37 solder joints which were formed by a std. convection oven attach of 30 mil (760 .mu.m) diam. **solder spheres** to org. soldering preservative OSP protected, **Cu** plated ball **pads** of an org. flip **chip** substrate. The ball pads are solder mask defined and of 0.635 mm nominal diam. (2) Flip **chip** bump pad solder joint consisting of 63/37 eutectic solder bumped **die** attached to a non-solder mask defined, OSP protected, **Cu** plated **pad** of the flip **chip** substrate. The flip **chip** bumps on the **die** are created by screen printing solder paste on the **die** pads and subsequent reflow attach, by a std. convection oven to the **die** under bump metallurgy (UBM). The nominal **die** UBM pad diam. is 0.085 mm. (3) Solder joint formed on a coupon which involved the reflow of the balls randomly placed on a Cu plated layer with no solder mask coating. The investigation was performed by first establishing the intermetallic growth rate at six different temps., ranging from 85.degree. to 150.degree.. The relation between intermetallic growth and time was shown to essentially follow the common parabolic diffusion relation to temp. esp. above 100.degree.. The activation energy (E.alpha.) and the growth const. (k0) were then calcd. from this data. The E.alpha. for the total intermetallic thickness was essentially similar for the three solder joint configurations of the ball, bump and the coupon described above. E.alpha. varied from 0.31 eV to 0.32 eV, while the K0 varied from 18.0 .mu.m/s1/2 to 24.2 .mu.m/s1/2.

RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L75 ANSWER 8 OF 47 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:630627 HCAPLUS
DN 137:298122
TI Electromigration studies of flip **chip** bump solder joints
AU Maeda, Akira; Umemura, Toshio; Sone, Takanoi; Nakagawa, Kazuyuki; Baba, Shinji; Nakanishi, Makoto; Abe, Takeshi
CS Advanced Technology R&D Center, Mitsubishi Electric Corp., 1-1-57 Miyashimo, 229-1195, Japan
SO Symposium on "Microjoining and Assembly Technology in Electronics" (2002), 8th, 309-314
CODEN: SMAEFT
PB Yosetsu Gakkai
DT Journal
LA Japanese
AB Electromigration causes several different kinds of failure on flip **chip** bumps. Metal ion behavior in the electromigration has been investigated for solder joints of the flip **chip** bumps. **Pb** atoms in the solder joints can migrate during electron flow at room temps. because the **Pb** atoms have a high migration rate. On the other hand, Cu and Ni atoms barely migrate as the electrons flow at the temps. higher than 125.degree.C. **Sn** atoms can also migrate at the same temps., however the transfer direction is opposite to Cu and Ni. It is shown that metal cracks caused by the electromigration depend on the migration rate of the **Pb**, Cu, Ni, and **Sn** atoms which vary with temps.

L75 ANSWER 9 OF 47 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:630624 HCAPLUS
DN 137:298119
TI Microstructure and soldering properties of CSP solder joints using **Sn**-Zn-Bi solder
AU Yamaguchi, Atsushi; Furusawa, Akio; Otani, Hiroyuki; Okeda, Junji; Iwanishi, Hiroaki; Hojo, Takashi; Hirose, Akio; Kobayashi, Kojiro F.
CS Matsushita Electric Industrial Co., Ltd., 2-7 Matsubacho, Kadoma, Osaka, Japan
SO Symposium on "Microjoining and Assembly Technology in Electronics" (2002), 8th, 295-300
CODEN: SMAEFT
PB Yosetsu Gakkai
DT Journal
LA Japanese
AB **BGA** and **chip**-size (CSP) packages have appeared to realize higher d. Printed Circuit Boards (PCBs) than QFP packages with products becoming more miniature and lightwt. Lead-free solder with a lower m.p. is desired to apply products which can not use **Sn**-**Ag**-Cu lead-free solder due to the limits of heat-tolerance of elec. components. We studied the soldering properties of CSP solder joints using Sn8Zn3Bi solder with a m.p. of 197 .degree.C. We detd. how the soldering conditions affected the solder joint properties by analyzing microstructure and mech. properties. We found that void formation was suppressed by a temp. profile that provided incomplete melting of **solder-balls** of CSPs, and Au/Ni plating on PCB pads resulted in joint quality deterioration compared to the **Cu pad**.

L75 ANSWER 10 OF 47 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:630591 HCAPLUS
DN 137:298096
TI Characterization of electroless Ni/Au under bump metals (UBMs) deposited on aluminum alloy pads and **solder bump** formation on the UBMs

AU Yamamoto, Yukihiro; Hashino, Eiji; Tatsumi, Kohei
CS Advanced Technology Res. Lab., Technical Development Bureau, Nippon Steel Corp., 20-1, Shintomi, Futtu-city Chiba-Prefecture, 293-8511, Japan
SO Symposium on "Microjoining and Assembly Technology in Electronics" (2002), 8th, 109-114
CODEN: SMAEFT
PB Yosetsu Gakkai
DT Journal
LA Japanese
AB The pretreatment process of aluminum pad for electroless deposition of Ni/Au was examd. in the zinc replacement method in acidic and alk. solns. There were morphol. differences on the surface of pretreated aluminum between the two methods. In the case of alk. soln., there was inhomogeneous deposition of Ni obsd. because of the island-like deposition of zinc as pretreatment. On the other hand zinc particles were smoothly deposited on acidic pretreated pure aluminum as well as Al-0.5 wt.% **Cu** alloy **pads**, resulting in the subsequent deposition of homogeneous Ni/Au. Eutectic SnPb **solder balls** of 100 .mu.m in diam. were mounted on the UBMs of 80 .mu.m square and reflowed at 230.degree.C. The shear strength of the **solder bumps** were over 60 gf/pin as av. By using our originally developed micro-ball mounter, **solder balls** were transferred onto the 385,000 UBMs formed on an 8 in. **wafer** and were successfully connected with the UBMs by reflow at 230.degree.C.

L75 ANSWER 11 OF 47 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:597628 HCAPLUS
DN 137:344699
TI Filter optimization for X-ray inspection of surface-mounted **ICs**
AU Blish, Richard C., II; Li, Susan X.; Lehtonen, David
CS Advanced Micro Devices, Sunnyvale, CA, 94088-3453, USA
SO IEEE International Reliability Physics Symposium Proceedings (2002), 40th, 377-379
CODEN: IIRPF9; ISSN: 1082-7285
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
AB A thin Zn filter (.apprxeq.20 .mu.m) and relatively low x-ray tube voltage (.apprxeq.45 kV) is recommended for x-ray inspection of surface-mounted device solder joints on printed wiring boards (PWB). An optimal filter minimizes the Si dose that could result in cumulative damage to sensitive **IC** circuit nodes, yet provides good contrast for **metals** such as **Cu** traces on PWB and device **solder balls**. While we expect orders of magnitude Si dose redns. when effective filters are inserted, a properly chosen filter should not attenuate the portion of the white x-ray spectrum required to image Cu, **Sn**, and **Pb** (**solder balls**). Some x-ray inspection suppliers can achieve a Si dose of as little as 0.060 Rads; while other x-ray inspection suppliers, not yet optimized for min. dose, may use as much as four orders of magnitude more dose. We used thermoluminescent detectors (TLDs) to measure the x-ray dose that **IC** product shipments would encounter during a shipping process (personal baggage or cargo) as minimal (.ltoreq.0.050 Rads).
RE.CNT 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L75 ANSWER 12 OF 47 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:570237 HCAPLUS
DN 137:282595
TI Fluxless bonding of **Sn**-3.5Ag **solder bump** flip **chip** by Ar+H2 plasma pre-treatment

AU Hong, Soon-Min; Kang, Choon-Sik; Jung, Jae-Pil
CS Micro-joining Lab., Samsung Electronics Co. Ltd., Suwon, 442-742, S. Korea
SO Taehan Kumsok, Chaeryo Hakhoechi (2002), 40(5), 562-567
CODEN: TKHABB
PB Korean Institute of Metals and Materials
DT Journal
LA Korean
AB Plasma treatment was applied to remove the surface oxide of **Sn** -3.5 wt.% Ag **solder bump** for fluxless flip **chip** bonding. The effects of plasma process parameters, such as plasma power, treatment time, chamber pressure, and H2 addn., on **Sn**-oxide etching characteristics were evaluated by Auger depth profile anal. The **die** shear tests were performed to evaluate the adhesion strength of **Sn**-3.5% Ag **solder bump** flip **chip**. The addn. of H2 to Ar plasma improved the oxide etching characteristics. A low chamber pressure was more effective in oxide removal. The **die** shear strength of the plasma-treated **Sn**-3.5Ag solder flip **chip** was higher than that of the non-treated **chip**, but it was lower than that of the fluxed **chip**. The difference in the **die** shear strength between the plasma-treated specimen and the non-treated specimen increased with increasing bonding temp. The plasma-treated flip **chip** fractured at the solder/TSM interface at low bonding temp., but at the solder/UBM interface at high bonding temp.

L75 ANSWER 13 OF 47 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:294714 HCAPLUS
DN 137:13888
TI Investigation of flip **chip** under bump **metallization** systems of **Cu pads**
AU Nah, Jae-Woong; Paik, Kyung-Wook
CS Department of Materials Science and Engineering, Korea Advanced Institute of Science and Technology, Taejon, 305-701, S. Korea
SO IEEE Transactions on Components and Packaging Technologies (2002), 25(1), 32-37
CODEN: ITCPFB; ISSN: 1521-3331
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
AB UBM material systems for flip **chip solder bumps** on **Cu pads** were studied using the electroless copper (E-Cu) and electroless nickel (E-Ni) plating methods; and the effects of the interfacial reaction between UBMs and **Sn** -36Pb-2Ag solders on the **solder bump** joint reliability were also studied to optimize UBM materials for flip **chip** on **Cu pads**. For the E-Cu UBM, scallop-like Cu6Sn5 intermetallic compd. (IMC) forms at the solder/E-Cu interface, and bump fracture occurred along this interface under a relatively small load. In contrast, at the E-Ni/E-Cu UBM, E-Ni serves as a good diffusion-barrier layer. The E-Ni effectively limited the growth of the IMC at the interface, and the polygonal-shape Ni3Sn4 IMC resulted in a relatively higher adhesion strength compared with the E-Cu UBM. As a result, electroless deposited UBM systems were successfully demonstrated as low cost UBM alternatives on **Cu pads**. The E-Ni/E-Cu UBM material system was a better choice for solder flip **chip** interconnection on **Cu pads** than the E-Cu UBM.
RE.CNT 17 THERE ARE 17 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L75 ANSWER 14 OF 47 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:141509 HCAPLUS

DN 136:271178
TI Eutectic **Sn-Ag solder bump** process for ULSI flip **chip** technology
AU Ezawa, Hirokazu; Miyata, Masahiro; Honma, Soichi; Inoue, Hiroaki; Tokuoka, Tsuyoshi; Yoshioka, Junichiro; Tsujimura, Manabu
CS Advanced Process Engineering Department, Toshiba Corporation Semiconductor Company, Yokohama, 235-8522, Japan
SO IEEE Transactions on Electronics Packaging Manufacturing (2001), 24(4), 275-281
CODEN: ITEPFL; ISSN: 1521-334X
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
AB A novel eutectic **Pb**-free **solder bump** process has been developed which provides several advantages over conventional **solder bump** processes. A thick plating mask can be fabricated for steep wall bumps using a nega-type resist with a thickness of more than 50 .mu.m by one time spin coating. This improves productivity for mass prodn. The two-step electroplating is performed using two sep. plating reactors for Ag and **Sn**. **Sn** layer is electroplated on Ag layer. Eutectic **Sn-Ag** alloy bumps can be easily obtained by annealing the Ag/**Sn** metal stack. This electroplating process does not need strict control of the content ratio of Ag to **Sn** in alloy plating solns. The uniformity of the reflowed bump height within a 6-in **wafer** was less than 10%. The Ag compn. range within a 6-in **wafer** was less than .+-.0.3 wt.% Ag at the eutectic **Sn-Ag** alloy, analyzed by ICP spectrometry. SEM observations of the interface of Cu/barrier layer/**Sn-Ag** solder and shear strength measurements of the **solder bumps** were performed after 5 times reflow at 260.degree. in N2 ambience. For the Ti(100 nm)/Ni(300 nm)/Pd(50 nm) barrier layer, the shear strength decreased to 70% due to the formation of **Sn**-Cu intermetallic compds. Thicker Ti in the barrier metal stack improved the shear strength. The thermal stability of Cu/barrier layer/**Sn-Ag** solder metal stack was examd. using Auger electron spectrometry anal. After annealing at 150.degree. for 1000 h in N2, **Sn** did not diffuse into Cu layer for Ti(500 nm)/Ni(300 nm)/Pd(50 nm) and Nb(300 nm)/Ti(100 nm)/Ni(300 nm)/Pd(50 nm) barrier metal stacks. These results suggest that the Ti/Ni/Pd barrier metal stack available to **Sn-Pb solder bump** and Au bump on Al pad is viable for **Sn-Ag solder bump** on **Cu pad** in upcoming ULSIs.
RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L75 ANSWER 15 OF 47 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:96674 HCAPLUS
DN 137:14203
TI Effect of **Cu stud** microstructure and electroplating process on intermetallic compounds growth and reliability of flip-**chip solder bump**
AU Xiao, Guo-Wei; Chan, Philip C. H.; Teng, Annette; Cai, Jian; Yuen, Matthew M. F.
CS Department of Electrical and Electronic Engineering, University of Science and Technology, Kowloon, Hong Kong
SO IEEE Transactions on Components and Packaging Technologies (2001), 24(4), 682-690
CODEN: ITCPFB; ISSN: 1521-3331
PB Institute of Electrical and Electronics Engineers
DT Journal

LA English
AB In electroplating-based flip-**chip** technol., the **Cu** **stud** and solder deposition processes are two of the most important factors affecting the reliability of solder joints. The growth of Cu-**Sn** intermetallic compds. (IMC) also plays a crit. role. In this paper, the effect of **Cu stud** surface roughness and microstructures on the reliability of solder joint was studied. The surface roughness of the **Cu stud** was increased as the Cu electroplating c.d. increased. The micro-structural morphol. of the Cu-**Sn** IMC layer was affected by **Cu stud** surface structure. We found the growth rate of IMC layer increased with the increasing of **Cu stud** grain size and surface roughness during aging test. The growth kinetics of Cu-**Sn** intermetallic compd. formation for 63Sn/37Pb solder followed the Arrhenius equation with activation energy varied from 0.78 ev to 1.14 ev. The ratios of Cu3Sn layer thickness to the total Cu-**Sn** IMC layer thickness was in the range of 0.5 to 0.15 for various Cu microstructures at 150.degree.C during thermal aging test. The shear strength of **solder bump** was measured after thermal aging and temp./humidity tests. The relationship between electroplating process and reliability of solder joints was established. The failure mode of solder joints was also analyzed.
RE.CNT 13 THERE ARE 13 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L75 ANSWER 16 OF 47 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:90494 HCAPLUS
DN 136:143759
TI Integrated power circuits with distributed bonding and current flow
IN Efland, Taylor R.; Pendharkar, Sameer
PA USA
SO U.S. Pat. Appl. Publ., 13 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002011674	A1	20020131	US 2001-917419	20010730
	JP 2002164437	A2	20020607	JP 2001-262416	20010727
PRAI	US 2000-221051P	P	20000727		

AB A semiconductor **integrated circuit** comprises contact pads located over active components, which are positioned to minimize the distance for power delivery between a selected pad and one or more corresponding active components, to which the power is to be delivered. This min. distance further enhances dissipation of thermal energy released by the active components. More specifically, a semiconductor **integrated circuit** comprises a laterally organized power transistor, an array of power supply contact pads distributed over the transistor, means for providing a distributed, predominantly vertical current flow from the contact pads to the transistor, and means for connecting a power source to each of the contact pads. Positioning the power supply contact pads directly over the active power transistor further saves precious Si real estate area. The means for vertical current flow include contact pads made of a stack of metal layers comprising refractory **metals** for adhesion, **Cu** and Ni as stress-absorbing metals, and Au or Pd as bondable and solderable outermost metals. The means for connecting a power source include wire bonding and **solder ball** interconnection.

L75 ANSWER 17 OF 47 HCAPLUS COPYRIGHT 2003 ACS

AN 2001:926184 HCAPLUS
DN 136:175991
TI Cr/**Cu**/Ni underbump **metalization** study
AU Leng, Tay Hui; Kirkpatrick, Galen; Tay, Andrew; Li, Lu
CS Institute of Microelectronics, Singapore Science Park 2, Singapore, 117685, Singapore
SO Proceedings - Electronic Components & Technology Conference (2001), 51st, 939-944
CODEN: PETCES
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
AB In flip-**chip** interconnection using eutectic **Pb/Sn solder bumps**, a highly reliable underbump metalization (UBM) is required to maintain adhesion and solder wettability. An exptl. study investigated the thermal stability of the Cr/Cu/Ni UBM - where Cr act as an adhesive, Cu a solder wettable layer and Ni a barrier. The process window for good thermal stability will reduce silicon cratering failure and intermetallic failure to ensure reliability. The Cu and Ni layers were varied in low, medium and high thickness to study their impact on **solder bump** strength and failure mechanisms. 5.times.3 Mm full array test **chips** (with Cr/Cu/Ni UBM) were subjected to thermal stability tests: (1) multiple reflow for 1.times., 5.times., 10.times., 20.times., and (2) high-temp. storage at 150.degree. up to 1000 h. The destructive ball shear test and cross-sectional anal. were done. Bump shear results show that the Cr/Cu/Ni UBM with Ni thickness (low to high) remains stable with respect to the no. of reflow cycles. The failures were cohesive (Mode I-within solder). A high Ni thickness inhibited Cu diffusion and suppressed Cu IMC formation at near the solder interface. Under-high temp. storage, intermetallic growth was accelerated and the excessive intermetallic formed was very brittle. For low Ni thickness, failure mode (Mode I + Mode II) was obsd. after aging (>500 h). The failure mode remained as cohesive in high Ni thickness UBM. For low to high thickness Cu mini-bumps, shear strength was maintained during multiple reflows and the shearing fracture remains within the solder. The failure mode shifted from Mode I (at t = 0) to Mode III interfacial failure (after aging) in Cr/low thickness Cu/medium thickness Ni UBM, when the limited Cu supply led to solder dewetting.
RE.CNT 9 THERE ARE 9 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L75 ANSWER 18 OF 47 HCAPLUS COPYRIGHT 2003 ACS
AN 2001:926177 HCAPLUS
DN 136:175990
TI Investigation of low cost flip **chip** under bump metallization (UBM) systems on **Cu pads**
AU Nah, Jae-Woong; Paik, Kyung-Wook
CS Dept. of Materials Science and Engineering MicroElectronic Packaging Lab.(MEPL), Korea Advanced Institute of Science and Technology, Taejon, 305-701, S. Korea
SO Proceedings - Electronic Components & Technology Conference (2001), 51st, 790-795
CODEN: PETCES
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
AB Cu is considered as a promising alternative interconnection material to Al-based interconnection materials in Si-based **integrated circuits** due to its low resistivity and superior resistance to the electromigration. New bumping and UBM material systems for solder flip

chip interconnection of **Cu pads** were studied using electroless-plated Cu (E-Cu) and electroless-plated Ni (E-Ni) plating methods as low cost alternatives. Optimally designed E-Ni/E-Cu UBM bilayer material system can be used not only as UBMs for **solder bumps** but also as bump itself. Electroless-plated E-Ni/E-Cu bumps assembled using anisotropic conductive adhesives on an org. substrate is successfully demonstrated and characterized.

RE.CNT 17 THERE ARE 17 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L75 ANSWER 19 OF 47 HCAPLUS COPYRIGHT 2003 ACS
AN 2001:926155 HCAPLUS
DN 136:192575
TI Thermal fatigue properties of lead-free solders on Cu and NiP under bump metallurgies
AU Zhang, Charles; Lin, Jong-Kai; Li, Li
CS Semiconductor Products Sector, Motorola Inc., Tempe, AZ, 85284, USA
SO Proceedings - Electronic Components & Technology Conference (2001), 51st, 463-470
CODEN: PETCES
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
AB Three **Pb**-free solders, SnCu0.7, SnAg3.8Cu0.7 and SnAg3.5 were evaluated on both electroless NiP and electroplated **Cu** under bump **metallurgies** (UBM) for flip **chip** applications. Eutectic SnPb37 solder was also evaluated as a baseline comparison with the **Pb**-free solders. Test **dice** with a size of 12.6.times.7.5 mm2 were direct flip **chip** attached to test boards with variety of solder alloy/UBM combinations. In order to accelerate **solder bump** fatigue, no underfill encapsulation was used on the assembled parts. Due to high CTE mismatch between the Si and PCB and low stand-off height of the flip **chip** assembly, conditions of 0 to 100.degree. and -40 to 125.degree. air-to-air thermal cycling were performed to maximize cycles to failure and to distinguish the fatigue life among the solder alloys/UBMs. The results showed that the SnCu0.7 solder, on both electroless NiP and electroplated Cu UBMs, had the longest thermal fatigue life among all the solder/UBM interconnect structures evaluated. The SnAg3.8Cu0.7 on electroplated Cu had a thermal fatigue life comparable to eutectic SnPb37 while SnAg3.5 on electroless NiP had the worst thermal fatigue life. The failure mechanism varied among the **Pb**-free solder/UBM combinations. The SnCu on both NiP and Cu UBMs had cohesive failure inside the **solder bump** due to extensive creep in this alloy during thermal cycling. Both SnAg3.5 on electroless NiP UBM and SnAg3.8Cu0.7 on electroplated Cu UBM showed fatigue cracks initiated and propagated through intermetallics and along the intermetallic/solder interfaces, resulting in a shorter thermal fatigue life. Based on these results, the SnCu0.7 solder alloy appears to be the best choice for **Pb**-free flip **chip** interconnect.

RE.CNT 14 THERE ARE 14 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L75 ANSWER 20 OF 47 HCAPLUS COPYRIGHT 2003 ACS
AN 2001:851773 HCAPLUS
DN 135:379722
TI **Wafer**-scale assembly of **chip**-size packages
IN Heinen, Katherine G.; Edwards, Darvin R.; Jacobs, Elizabeth G.
PA USA
SO U.S. Pat. Appl. Publ., 17 pp.
CODEN: USXXCO

DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2001044197	A1	20011122	US 1998-186973	19981105
PRAI	US 1998-186973		19981105		

AB A **wafer**-scale assembly app. for **integrated circuits** and a method for forming the **wafer**-scale assembly are disclosed. A semiconductor **wafer** including a plurality of circuits is provided with a plurality of metal contact pads as elec. entry and exit ports. A 1st **wafer**-scale patterned polymer film carrying **solder balls** for each of the contact pads on the **wafer** is positioned opposite the **wafer** and the film are aligned. The film is brought into contact with the **wafer**. Radiant energy in the near IR spectrum is applied to the backside of the **wafer**, heating the **wafer** uniformly and rapidly without moving the semiconductor **wafer**. Thermal energy is transferred through the **wafer** to the surface of the **wafer** and into the **solder balls**, which reflow onto the contact pads, while the thermal stretching of the polymer film is mech. compensated. The uniformity of the height of the liq. **solder balls** is controlled either by mech. stoppers or by the precision linear motion of motors. After cooling, the **solder balls** solidify and the 1st polymer film is removed. The process is repeated for assembling sequentially a **wafer**-scale patterned interposer overlying all of the **solder balls** and the **wafer** and contacting each **solder ball** with a soldered joint, and a 2nd **wafer**-scale patterned film carrying **solder balls** contacting the interposer. In each process, the **wafer** is heated uniformly and rapidly and without moving it, the alignment is maintained during heating by mech. compensating for the thermal stretching of the polymer film, and the uniformity of the height of the liq. **solder balls** is controlled by mech. stoppers or position closed-loop linear actuators. The 2nd film is removed after cooling. Other embodiments are also disclosed.

L75 ANSWER 21 OF 47 HCAPLUS COPYRIGHT 2003 ACS
AN 2001:715843 HCAPLUS
DN 136:13883
TI Development of an etchant for selectively etching TiWNx in the presence of electroplated 95% **Pb**-5% **Sn** solder
AU Ramanathan, Lakshmi N.; Mitchell, Doug
CS Final Manufacturing Technology Center, Motorola, Inc., Chandler, AZ, 85224, USA
SO IEEE Transactions on Components and Packaging Technologies (2001), 24(3), 425-430
CODEN: ITCPFB; ISSN: 1521-3331
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
AB Shrinking **die** sizes and increasing I/O d. is motivating the push toward flip **chip** packages. A flip **chip** interconnection system with a under bump metallurgy stack contg. sputtered TiWNx/sputtered **Cu**/electroplated **Cu stud** /electroplated 95%**Pb**-5%**Sn** was developed. An important step in the above process is the selective etching of the sputtered Cu bus layer and the TiWNx barrier layer, in the presence of the **Pb**-**Sn** solder. The Cu bus layer was selectively etched using com. etchants. However, no com. etchants were available for selectively

etching the TiWNx layer. H2O2-NH4OH based etching systems, popularly known as Std. Clean-1 cleaning solns., were extensively used to clean Si **wafers** in front end **wafer** fabrication where only trace metal contamination exists. Since **metals** like lead, **Cu**, Ti, **Sn** and tungsten catalyze the heterogeneous decompn. of the peroxide, the unstable H2O2-NH4OH based etching systems are rarely used to etch metal films. The development of a H2O2-NH4OH based etchant to selectively etch the sputtered TiWNx films in the presence of electroplated 95%**Pb**-5%**Sn solder bumps** is discussed. A 23 full factorial expt. with mid point was conducted to establish the etchant compn., as well as process temp., that give satisfactory responses with respect to etch time, permissable undercut of the **Cu stud** (caused by the NH4OH), and acceptable bump shape after reflow. Statistical anal. was used to understand the significant factors influencing the etch rate and undercut. An etchant contg. 6% by vol. of 30%-H2O2 and 0.75% by vol. of 30%-NH4OH operated at a temp. of 37.degree. gave satisfactory results.

RE.CNT 22 THERE ARE 22 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L75 ANSWER 22 OF 47 HCAPLUS COPYRIGHT 2003 ACS
AN 2001:622138 HCAPLUS
DN 135:311328
TI Ethylene glycol ether free solder paste development
AU Lytle, Bill; Fang, Treliant; Li, Li; Zhang, Charles
CS Semiconductor Products Sector, Motorola, Tempe, AZ, 85284, USA
SO Journal of Electronic Materials (2001), 30(8), 1035-1041
CODEN: JECMA5; ISSN: 0361-5235
PB Minerals, Metals & Materials Society
DT Journal; General Review
LA English
AB A review with refs. There are growing concerns in the electronics industry for not only finding alternatives to lead but also other potentially hazardous materials as well. This paper summarizes the development of ethylene glycol ether (EGE)-free solder flux for the formulation of **Pb**-free solder pastes. Replacing the toxic components in the flux was only the 1st challenge, the criteria of com. proven pastes also had to be met. Both com. and inhouse solder paste formulations were evaluated for printability, reflow, wetting, flux residue removal, and solder void characteristics. Two crit. issues, **solder bump** voids and flux residue removal, were identified and assocd. with the high temp. reflow of **Pb**-free pastes. These issues were not effectively improved by the existing com. EGE-free solder pastes. New solder paste formulations were developed using alternative chem. than those found in traditional solder paste fluxes. These pastes, some of which are also water sol., reduced void frequency and size by >4x as compared to vendors' pastes. **Solder bump** height uniformity of 135 .+-. 4 .mu.m within each **die** was consistently achieved. Thermal-mech. reliability tests were performed on various **Pb**-free solder alloys using the new flux formulations. The reliability of flip **chip** assembled DCA on org. boards with both OSP/Cu and **Cu**/Ni/Au **pad** metalizations were comparable to eutectic Sn63Pb37 bumped assemblies using com. pastes.

RE.CNT 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L75 ANSWER 23 OF 47 HCAPLUS COPYRIGHT 2003 ACS
AN 2001:246852 HCAPLUS
DN 134:274435
TI Semiconductor devices having **copper pads** and

fabrication thereof
IN Honma, Soichi; Miyata, Masahiro; Ezawa, Hirokazu
PA Toshiba Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 11 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2001093928	A2	20010406	JP 1999-269272	19990922
TW 468245	B	20011211	TW 2000-89117652	20000830

PRAI JP 1999-269272 A 19990922

AB The title devices have semiconductor components packaged on a **solder bump** provided via a **Cu pad** on a circuit board. The title fabrication involves forming on the **Cu pad** with a **Cu**-diffusion preventive barrier metal film such as a Ti/Ni/Pd film and providing a metal bump contact or metal wire for mounting semiconductor packages. The use of the diffusion barriers effectively prevents Cu diffusion to the bump contacts in prevention of interface delamination in mounting packages.

L75 ANSWER 24 OF 47 HCAPLUS COPYRIGHT 2003 ACS
AN 2001:66870 HCAPLUS
DN 134:196500
TI Interfacial reaction between electroless-plated UBM (under bump **metallurgy**) on **Cu pads** and **Pb-Sn-Ag solder bumps**
AU Nah, Jae-Woong; Paik, Kyung-Wook
CS Dept. of Material Science and Engineering, Korea Advanced Institute of Science and Technology, Taejon, Yusung-gu, Kusung-dong, 305-701, S. Korea
SO Han'guk Chaelyo Hakhoechi (2000), 10(12), 853-863
CODEN: HCHAEU; ISSN: 1225-0562
PB Materials Research Society of Korea
DT Journal
LA Korean
AB A UBM system for solder flip **chip** interconnection of **Cu pads** was investigated by using the electroless copper and electroless Ni-P plating method. The interfacial reaction between several UBM structures and **Sn**-36Pb-2Ag solder and its effect on **solder bump** joint mech. reliability were investigated to optimize the UBM design for **solder bump** on **Cu pads**. For the electroless Cu UBM, continuous coarse scallop-like Cu6Sn5 intermetallic compd. was formed at the solder/Cu interface, and bump fracture occurred at this interface under a relative low load. In contrast, For the electroless Ni-P/electroless Cu UBM, the electroless Ni-P effectively limited the growth of Cu6Sn5 at the interface, and polygonal Ni3Sn4 was formed because of the crystallog. mismatch between monoclinic Ni3Sn4 and amorphous electroless Ni-P phase. Consequently, a relatively higher bump adhesion strength was obsd. at electroless Ni-P/electroless Cu UBM than the electroless Cu UBM. Therefore the electroless Ni-P/electroless Cu UBM system was a better choice for solder flip **chip** interconnection on **Cu pads**.

L75 ANSWER 25 OF 47 HCAPLUS COPYRIGHT 2003 ACS
AN 2001:22747 HCAPLUS
DN 134:200907
TI Eutectic **Sn-Ag solder bump** process for ULSI flip-**chip** technology
AU Ezawa, Hirokazu; Miyata, Masahiro; Honma, Soichi; Inoue, Hiroaki; Tokuoka, Tsuyoshi; Yoshioka, Junichiro; Tsujimura, Manabu

CS Advanced Process Engineering Department, Toshiba Corporation Semiconductor Company, Yokohama, 235-8522, Japan
SO Proceedings - Electronic Components & Technology Conference (2000), 50th, 1095-1100
CODEN: PETCES
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
AB The newly developed **Sn-Ag** eutectic **solder bump** process provides several advantages over conventional **solder bump** process schemes. Steep wall bumps as plated were fabricated using a nega-type photoresist with a thickness of more than 50 .mu.m by one time spin coating. This improves productivity for mass prodn. The 2-step electroplating process was performed using sep. plating reactors for the Ag and **Sn**. The eutectic **Sn-Ag** alloy bumps were easily obtained by annealing the metal stacks with **Sn** layer on Ag layer sequentially electroplated. This electroplating process does not need strict control of the content ratio of Ag to **Sn** in an alloy plating soln. even with increasing electroplating depositions. The novel developed process gives the within-**wafer** uniformity of the bump height as reflowed of less than 10% and of the **Sn-Ag** alloy compn. as reflowed of less than .+-.0.5 wt.% Ag, analyzed by ICP spectrometry. Shear strength measurements were performed to know the thermal stability for the structure of **Cu pads**/Ti/Ni/Pd/**Sn-Ag** eutectic solder stack. In the case of Ti (100 nm)/Ni (300 nm)/Pd (50 nm) barrier metal stacks, the shear strength after 5 times annealing in a N2 ambience at 260.degree. decreased to 70% than that as reflowed. As the Ti becomes thicker in the Ti/Ni/Pd metal stack, shear strengths are improved. Comparing the structure of Cu/Ti/Ni/Pd/**Sn-Ag** eutectic solder with those of Ta/Ti/Ni/Pd and Nb/Ti/Ni/Pd barrier metal stacks, the anal. results of Auger spectrometry show that **Sn** diffusion into Cu to form Cu-**Sn** alloy was obsd. only in Cu/Ta/Ti/Ni/Pd barrier metal stacks. These results suggest that the same Ti/Ni/Pd barrier metal stack as used in **Sn-Pb solder bump** and Au bump is viable for ULSIs with Cu interconnects.
RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L75 ANSWER 26 OF 47 HCAPLUS COPYRIGHT 2003 ACS
AN 2001:22702 HCAPLUS
DN 134:201398
TI Development of an etchant for selectively etching TiWNx in the presence of electroplated 95% **Pb**-5% **Sn** solder
AU Ramanathan, Lakshmi N.; Mitchell, Doug
CS Final Manufacturing Technology Center, Motorola Inc., Chandler, AZ, 85224, USA
SO Proceedings - Electronic Components & Technology Conference (2000), 50th, 837-843
CODEN: PETCES
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
AB Shrinking **die** sizes and increasing I/O d. is motivating the push towards flip **chip** packages. A flip **chip** interconnection system with a under bump metallurgy stack contg. sputtered TiWNX/sputtered **Cu**/electroplated **Cu stud** /electroplated 95%**Pb**-5%**Sn** was developed. An important step in the above process is the selective etching of the sputtered Cu bus layer and the TiWNX barrier layer, in the presence of the **Pb-Sn** solder. The Cu bus layer was selectively etched using com.

etchants. However, no com. etchants were available for selectively etching the TiWNX layer, H2O2-NH4OH based etching systems, popularly known as Std. Clean-1 cleaning solns., were extensively used to clean Si **wafers** in front end **wafer** fabrication where only trace metal contamination exists. Since **metals** like lead, **Cu**, Ti, **Sn** and tungsten catalyze the heterogeneous decompn. of the peroxide, the unstable H2O2-NH4OH based etching systems are rarely used to etch metal films. The development of a H2O2-NH4OH based etchant to selectively etch the sputtered TiWNX films in the presence of electroplated 95%**Pb**-5%**Sn solder bumps** is discussed. A 23 full factorial expt. with mid point was conducted to establish the etchant compn., as well as process temp., that give satisfactory responses with respect to etch time, permissable undercut of the **Cu stud** (caused by the NH4OH), and acceptable bump shape after reflow. Statistical anal. was used to understand the significant factors influencing the etch rate and undercut. An etchant contg. 6% by vol. of 30%-H2O2 and 0.75% by vol. of 30%-NH4OH operated at a temp. of 37.degree. gave satisfactory results.

RE.CNT 21 THERE ARE 21 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L75 ANSWER 27 OF 47 HCAPLUS COPYRIGHT 2003 ACS
AN 2001:22593 HCAPLUS
DN 134:215363
TI The effect of **Cu stud** structure and eutectic solder electroplating on intermetallic growth and reliability of flip-**chip solder bump**
AU Xiao, Guowei; Chan, Philip; Jian, Cai; Teng, Annette; Yuen, Matthew
CS Department of Electrical and Electronic Engineering, Hong Kong University of Science and Technology, Hong Kong SAR, Peop. Rep. China
SO Proceedings - Electronic Components & Technology Conference (2000), 50th, 54-59
CODEN: PETCES
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
AB In electroplating-based flip-**chip** technol., the **Cu stud** and solder deposition process is one of the most important factors affecting the reliability of solder joints. The growth of Cu-**Sn** intermetallic compds. (IMC) also plays a crit. role. The effect of **Cu stud** surface roughness and microstructures on the reliability of solder joint was studied. The micro-structural morphol. of the Cu-**Sn** IMC layer was affected by **Cu stud** surface structure. The **Cu stud** with sloped edge can impacted the adhesion of **solder bump** and UBM (Under Bump Metallurgy) layer. Insufficient solder wetting at edge of the **Cu stud** can further degrade the reliability of solder joints. The authors obsd. the thickness of -phase Cu6Sn5 layer increased continuously instead of -phase Cu6Sn5 due to the deficiency of **tin** at the bottom of **solder bump** after extended thermal aging. The adhesion of **Cu stud** and UBM layer was weakened due to the growth of Cu3Sn at the edge of **Cu stud**. Both of the Cu-**Sn** IMC layers grew at the top of **Cu stud** as the aging time increased. The mean thickness of two IMC layers increased linearly with the square root of aging time. Cracks formed easily at the interface of Cu-**Sn** IMC layer and **solder bump**, esp. at the **Pb**-rich layer and IMC layer interface. Cracks led to low bump shear strength after extended thermal aging. The authors did not observe cracks formed at the Cu6Sn5 and Cu3Sn interface. The SEM and EDAX anal. suggested that the fracture surface structure was influenced by the

Cu stud microstructure and **solder bump** deposition process.
RE.CNT 12 THERE ARE 12 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L75 ANSWER 28 OF 47 HCAPLUS COPYRIGHT 2003 ACS
AN 2000:90608 HCAPLUS
DN 132:230119
TI Shearing strength and materials interaction during reflow of Al/Cu/Electroless Nickel/**solder bump**
AU Lin, Kwang-Lung; Liu, Yi-Cheng
CS Department of Materials Science and Engineering, National Cheng Kung University, Tainan, 701, Taiwan
SO Proceedings - Electronic Components & Technology Conference (1999), 49th, 607-612
CODEN: PETCES
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
AB 63Sn-37Pb **solder bump** was produced on Al terminal of Si. The bump pad dimension is 100.mu.m .times. 100.mu.m while the pitch size is 250 .mu.m. The bump pattern contains 20 .times. 20 bumps. The UBM (under bump **metallurgy**) consists of **Cu**/Electroless Nickel. Cu was sputtering deposited on Al film. The **solder bump** was electroplated on the electroless nickel followed by reflow at 210.degree.C or 250.degree.C. The reflow was conducted for 1, 5, and 10 cycles. Intermetallic compds. Ni3Sn2, Ni3Sn4, and Ni4Sn were formed between electroless nickel plating and solder when reflowed at 250.degree.C. The interdiffusion behavior of the **solder bump** constituents within the **solder bump** was investigated by scanning electron microscope (SEM). Cu was found to penetrate the electroless nickel during reflow when the thickness of the electroless nickel plating is only 1.8 .mu.m. No penetration of Cu occurs through a 10 .mu.m electroless nickel during reflow. **Sn** and Al were not found to diffuse through the electroless nickel during reflow even for 1.8 .mu.m of electroless nickel plating. The shearing strength of the **solder bump** reflowed at 210.degree.C is 53.5.+-.3.3 g/bump while the shearing strength is 62.9.+-.2.8 g/bump when reflowed at 250.degree.C. The fracture after shearing test occurs within the solder. Repeating reflow tends to lower the shearing strength of the bump. The shearing strength of the bump becomes 37.6.+-.6.0 g/bump after ten cycles of reflow.
RE.CNT 11 THERE ARE 11 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L75 ANSWER 29 OF 47 HCAPLUS COPYRIGHT 2003 ACS
AN 2000:90599 HCAPLUS
DN 132:230112
TI Solder metalization interdiffusion in **microelectronic** interconnects
AU Zribi, A.; Chromik, R. R.; Presthus, R.; Clum, J.; Teed, K.; Zavalij, L.; De Vita, J.; Tova, J.; Cotts, E. J.
CS State University of New York at Binghamton Physics Department, Binghamton, NY, 13902, USA
SO Proceedings - Electronic Components & Technology Conference (1999), 49th, 451-457
CODEN: PETCES
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
AB We investigated intermetallic compd. formation mechanisms and their effect

on the integrity of **ball grid** array Cu/Ni/Au/solder joints integrity. Substrates with three types of Au plating, and thus three different thicknesses [electrolytic (2.6 and 0.75 .mu.m), immersion (0.25 .mu.m), and selective (0.02 .mu.m)] were used. After solder reflow, the solder joints were annealed for up to 1000 h at 150.degree.C. Optical and electronic metallog. together with Energy Dispersive Spectroscopy were used to locate and identify phases present in the joint for different annealing times. Brittle failure of solder joints was ascribed to the formation of a ternary intermetallic (Au0.5Ni0.5)Sn4 at the interface solder/substrate. In the absence of post-reflow thermal aging, only Ni3Sn4 was obsd. at the interface and it did not decrease the mech. reliability of the joint. Tensile-shear stress tests were performed on unaged samples as well as samples aged for 1 h, 4 h and 450 h.

RE.CNT 9 THERE ARE 9 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L75 ANSWER 30 OF 47 HCAPLUS COPYRIGHT 2003 ACS
AN 1999:736357 HCAPLUS
DN 132:57615
TI Reaction kinetics of **solder-balls** with pads in **BGA** packages during reflow soldering
AU Ho, C. E.; Chen, Y. M.; Kao, C. R.
CS Department of Chemical Engineering, National Central University, Chungli, Taiwan
SO Journal of Electronic Materials (1999), 28(11), 1231-1237
CODEN: JECMA5; ISSN: 0361-5235
PB Minerals, Metals & Materials Society
DT Journal
LA English
AB The Au/Ni/Cu three-layer structure is one of the most common **solder-ball** pad finishes for the **ball-grid**-array (**BGA**) packages. The 1st layer, which is to be in direct contact with the solder, is a 1-.mu.m Au layer. Beneath the Au layer is the Ni layer, whose thickness is .apprx.7 .mu.m. The Cu layer is part of the internal wiring of a **BGA** package. Eutectic PbSn **solder-balls** were reflowed on the Au/Ni/**Cu pads** at 225.degree. for reflow times from 7.5 s to 1003 s. The Au layer reacted very quickly with the solder to form AuSn4 and AuSn2. The growth rate of AuSn4 + AuSn2 was very high, approaching 1 .mu.m/s. When the reflow time reached 10 s, all the Au had been consumed, and AuSn2 had been converted to AuSn4. Also, AuSn4 grains began to sep. themselves from the Ni layer at the roots of the grains, and started to fall into the solder. When the reflow time reached 30 s, all AuSn4 grains had left the interface and a thin layer of Ni3Sn4 formed at the solder-Ni interface. The growth rate of this Ni3Sn4 layer was very low, reaching only 6 .mu.m for 1003 s of reflow. During reflow the Au layer reacted with **Sn** to form AuSn4 1st, and then broke off and fell into the molten solder. The Au layer did not dissolve into the molten solder directly during reflow.

RE.CNT 18 THERE ARE 18 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L75 ANSWER 31 OF 47 HCAPLUS COPYRIGHT 2003 ACS
AN 1999:736354 HCAPLUS
DN 132:57614
TI Kinetics of copper and high **Pb**/high **Sn** bilayered **Pb-Sn** solder interactions
AU Zuruzi, A. S.; Chiu, C.-H.; Lahiri, S. K.; Chua, K. M.
CS Institute of Materials Research and Engineering, Singapore, 119260, Singapore
SO Journal of Electronic Materials (1999), 28(11), 1224-1230

CODEN: JECMA5; ISSN: 0361-5235
PB Minerals, Metals & Materials Society
DT Journal
LA English
AB Use of bilayered **Pb-Sn** solders consisting of high **Sn** and high **Pb** solder compns. is an option for joining **chips** to org. substrates at lower temps. in which the high **Sn** solder is deposited onto **Cu pads** on the substrates. In this work interactions between the two-layered solder and **copper pads** during the reflow operation were studied for both flip **chip** and **Ball Grid** Array (**BGA**) applications. **Sn** from the high **Sn** solder migrates faster at the edges along the surface of the high **Pb** solder than at the interior, resulting in a nonuniform **Sn** concn. along the Cu-solder interface. The thickness of the intermetallic compd. formed due to the interaction of Cu and **Sn** also is nonuniform along the solder-Cu interface. This was attributed to the variation in the **Sn** concn. of the solder adjacent to the **Cu pads** at different positions. The intermetallic compd. growth rate was explained using a model based on **Sn** diffusion into copper.
RE.CNT 19 THERE ARE 19 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L75 ANSWER 32 OF 47 HCAPLUS COPYRIGHT 2003 ACS
AN 1999:313359 HCAPLUS
DN 131:76862
TI Studies on the interfacial reaction between electroplated eutectic **Pb/Sn** flip-**chip solder bump** and UBM (under bump metallurgy)
AU Jang, Se-Young; Paik, Kyung-Wook
CS Dep. of Mater. Sci. and Eng., Korea Advanced Inst. of Sci. and Technol., Taejon, 305-701, S. Korea
SO Han'guk Chaelyo Hakhoechi (1999), 9(3), 288-294
CODEN: HCHAEU; ISSN: 1225-0562
PB Materials Research Society of Korea
DT Journal
LA Korean
AB In the flip **chip** interconnection using **solder bumps**, the Under Bump Metallurgy (UBM) is required to perform multiple functions in its conversion of an Al bond pad to a solderable surface. In this study, various UBM systems such as Al1.mu.m/Ti0.2.mu.m/Cu5.mu.m, Al1.mu.m/Ti0.2.mu.m/Cu1.mu.m, Al1.mu.m/Ni0.2.mu.m/Cu1.mu.m and Al1.mu.m/Pd0.2.mu.m/Cu1.mu.m for flip **chip** interconnection using the low m.p. eutectic 63Sn-37Pb solder were investigated and compared to their metallurgical properties. 100 .mu.M size bumps were prepd. using an electroplating process. The effects of the no. of reflows and aging time on the growth of intermetallic compds. (IMC) were investigated. Cu6Sn5 and Cu3Sn IMC were obsd. after aging treatment in the UBM system with thick copper (Al 1 .mu.m/Ti 0.2 .mu.m/Cu 5 .mu.m). However only the Cu6Sn5 was detected in the UBM systems with 1 .mu.m thick Cu even after 2 reflows and 7 day aging at 150.degree.C. Complete Cu consumption by Cu-**Sn** IMC growth gives rise to a direct contact between solder inner layer such as Ti, Ni, and Pd, and hence to possibly cause reactions between two of them. In this study, however, only for the Pd case, IMC of PdSn4 was obsd. by Cu consumption. UBM interfacial reactions with solder affected the adhesion strength of **solder balls** after solder reflow and annealing treatment.

L75 ANSWER 33 OF 47 HCAPLUS COPYRIGHT 2003 ACS
AN 1999:204845 HCAPLUS

DN 130:315043
TI Direct correlation between mechanical failure and metallurgical reaction in flip **chip** solder joints
AU Liu, C. Y.; Chen, Chih; Mal, A. K.; Tu, K. N.
CS Department of Materials Science and Engineering, UCLA, Los Angeles, CA, 90095, USA
SO Journal of Applied Physics (1999), 85(7), 3882-3886
CODEN: JAPIAU; ISSN: 0021-8979
PB American Institute of Physics
DT Journal
LA English
AB We tested flip **chip** solder bonded Si specimens under tensile and shear loading as a function of annealing time at 200 .degree.C. The **solder bump** was eutectic SnPb and the underbump thin film **metalization** was **Cu**/Cr deposited on oxidized Si. The failure mode is interfacial fracture and the fracture strength decreases rapidly with annealing time. From SEM observations, the fracture occurs at the Cu-**Sn**/Cr interface. We conclude that it is the metallurgical reaction that has brought the solder into direct contact with the Cr surface. The weak joint is due to the spalling of Cu-**Sn** compd. grains from the Cr surface, esp. near the edges and corners of the joint.
RE.CNT 11 THERE ARE 11 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L75 ANSWER 34 OF 47 HCAPLUS COPYRIGHT 2003 ACS
AN 1998:671670 HCAPLUS
DN 129:292513
TI Under bump metalization development for eutectic **Pb-Sn** solders
AU Hong, S. J.; Korhonen, T. M.; Korhonen, M. A.; Li, C.-Y.
CS Department of Materials Science and Engineering, Cornell University, Ithaca, NY, 14850, USA
SO Materials Research Society Symposium Proceedings (1998), 515(Electronic Packaging Materials Science X), 73-77
CODEN: MRSPDH; ISSN: 0272-9172
PB Materials Research Society
DT Journal
LA English
AB Due to its advantage in no. of I/Os over other interconnection method, flip **chip** interconnection technol. plays a key role in today's electronics packaging. Good understanding of interfacial reactions between the **solder balls** and under bump metalizations (UBM) is crucial in producing sound and reliable solder joints. In the present paper, several new under bump metalization (UBM) schemes using Ni or CuNi alloys as solderable layer are investigated. Cr or Ti is used as the adhesion layer. Test joint are made by re-flowing eutectic **Pb -Sn solder balls** on UBMs and through the use of SEM and micromech. shear testing, the reliability of the UBM scheme is detd. Exptl. result shows that some of the new schemes, featuring CuNi wettable layer with Cr or Ti adhesion layer produce reliable joints.
RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L75 ANSWER 35 OF 47 HCAPLUS COPYRIGHT 2003 ACS
AN 1998:567193 HCAPLUS
DN 129:268450
TI Under bump metalization development for high **Sn** solders
AU Korphonen, T. M.; Hong, S. J.; Su, P.; Zhou, C.; Korhonen, M. A.; Li, C.-Y.
CS Department of Materials Science and Engineering, Cornell University,

Ithaca, NY, 14853, USA
SO Materials Research Society Symposium Proceedings (1998), 505(Thin-Films--Stresses and Mechanical Properties VII), 143-148
CODEN: MRSPDH; ISSN: 0272-9172
PB Materials Research Society
DT Journal
LA English
AB Several under bump metalization (UBM) schemes using Ni or CuNi alloys as the solderable layer were investigated. Cr or Ti was used as the adhesive layer. UBM pads of different compns. were sputter-deposited on silicon **wafers** and patterned using std. photolithog. processes. Eutectic **Sn-Pb solder balls** were reflowed on top of the pads. The resulting interfacial microstructures were examd. by SEM/EDX spectroscopy anal. of cross-sectioned samples. The integrity of the UBM/solder interface was characterized by micromech. shear testing of flip **chip** test samples. Growth of intermetallic layers was found to be significantly slower in Ni and CuNi schemes compared to pure Cu. The joints on Ni and CuNi had also better adhesion at the UBM/solder interface, and in the shear tests the fracture occurred through the solder.
RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L75 ANSWER 36 OF 47 HCAPLUS COPYRIGHT 2003 ACS
AN 1998:439835 HCAPLUS
DN 129:223852
TI **Solder bump** fabrication on **wafers** by electroplating process
AU Watanabe, S.; Ihara, Y.; Kitahara, Y.; Kobayashi, T.; Wakabayashi, S.
CS Material & Process Reseach & Development Div., RandD Dept., Shinko Electric Industries Co., Ltd., Nagano, 381-22, Japan
SO IEMT/IMC Symposium, 1st, Sonic City-Omiya, Japan, Apr. 16-18, 1997 (1997), 110-115 Publisher: SHM: The Microelectronics Society, Tokyo, Japan.
CODEN: 66JZAY
DT Conference
LA English
AB **Wafer** Bumping process for flip **chip** interconnect was developed using sputtering and electroplating technologies. The process was composed of UBM(Under-Bump Metallurgy) layer fabrication and following photoresist imaging and solder electroplating processes. For the UBM **metals**, Ti, Cr, **Cu**, Ni and Au were evaluated as an adhesion layer, barrier layer and oxidn. or chem. attack protection layer for solder plating. In this case, Ti, Cr and Cu were sputtered as seeding layers for plating and thicker Cu Ni and Au were electroplated. The photoresist used in this process was 100.mu.m thick dry films composed of two layers on a **wafer**. The compns. of **solder bumps** were 10Sn/90Pb and eutectic, and those were well controlled by maintaining the **Sn/Pb** concns. and ratio in the plating solns. properly. In ordinary case, the compn. differences between bumps and plating solns. were less than +/-2%. Plated **solder bumps** were keeping column shape instead of mushroom shape obtained in thin photoresist case. This is advantageous to control the bump height and realize the fine pitch **solder bumps** on **wafers** compared with mushroom bumps. After stripping the photoresist, the bumps were reflowed with flux to obtain round shape bumps. Plating equipment was also specially designed to achieve high throwing power and uniform bump height on all over the **wafer**. The characteristics of bumps such as shape, height distribution, shear strength, elec. resistance and reliability after (T/C,HTS and Reflow test) were also evaluated.
RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD

ALL CITATIONS AVAILABLE IN THE RE FORMAT

L75 ANSWER 37 OF 47 HCAPLUS COPYRIGHT 2003 ACS
AN 1998:439638 HCAPLUS
DN 129:209921
TI Batch transfer of microstructures using flip-**chip solder bump** bonding
AU Singh, Angad; Horsley, David A.; Cohn, Michael B.; Pisano, Albert P.; Howe, Roger T.
CS Berkeley Sensor & Actuator Center, University of California at Berkeley, Berkeley, CA, 94720-1774, USA
SO Transducers 97, International Conference on Solid-State Sensors and Actuators, Chicago, June 16-19, 1997 (1997), Volume 1, 265-268 Publisher: Institute of Electrical and Electronics Engineers, New York, N. Y. CODEN: 66KBAZ
DT Conference
LA English
AB This paper describes a novel method for transfer and assembly of microstructures using sacrificial-layer micromachining and flip-**chip** bonding. The technique was performed at room temp. (cold weld) and at the back end of the process flow, and may thus provide a com. viable alternative to monolithic integration and costly hybrid packages. The transfer is achieved using break-away tethers and by cold welding electroplated In **solder bumps** to thick electroplated **Cu pads**. Both high aspect ratio MEMS devices as well as surface micromachined devices were successfully transferred using this method with no observable misalignment between moving and stationary parts. The ultimate tensile and shear strength of the solder bond is 11 .+-. 3 MPa and 9 .+-. 1 MPa resp. The contact resistance is of the order of 1.5 m.OMEGA. for a 65 .mu.m .times. 65 .mu.m .times. 4 .mu.m In bump.
RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L75 ANSWER 38 OF 47 HCAPLUS COPYRIGHT 2003 ACS
AN 1997:713697 HCAPLUS
DN 128:55786
TI Microstructure and reliability of sputter deposited Cr-CrCu-Cu thin films for flip-**chip** applications
AU Zhang, N. A.; Mcnicholas, Mark; Colvin, Neil
CS Applications Laboratory, Materials Research Corporation, Orangeburg, NY, 10962, USA
SO Materials Research Society Symposium Proceedings (1997), 445(Electronic Packaging Materials Science IX), 9-14 CODEN: MRSPDH; ISSN: 0272-9172
PB Materials Research Society
DT Journal
LA English
AB The Cr-CrCu-**Cu metal** scheme, as a terminal multistructure metalization for flip **chip** applications, was studied using PVD sputter deposition varying the conditions of deposition power and temp., and film thickness. A modified Controlled Collapse **Chip** Connection (C4) process was used to evaluate the aforementioned deposition of the Cr-CrCu-Cu multilayers and the effect of film microstructure on the parameters of shear strength and thermal cycle reliability. Thermal cycle reliability results proved to be a function of both the CrCu alloy and the Cu overlayer thickness. TEM cross sections of the Cr-CrCu-Cu multilayers suggests that the columnar grain structure of the CrCu layer may provide a sacrificial thermal diffusion barrier between the PbSn alloy **solder balls** and the Al bond pads during the thermal-cycle tests.

L75 ANSWER 39 OF 47 HCAPLUS COPYRIGHT 2003 ACS
AN 1997:97747 HCAPLUS
DN 126:147188
TI Forming a **solder bump** on small **copper pad** by fusion impact of an ejected microdroplet
IN Melton, Cynthia M.; Pfahl, Robert
PA Motorola, Inc., USA
SO U.S., 5 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 5597110	A	19970128	US 1995-519439	19950825
PRAI US 1995-519439		19950825		

AB The **Cu pad** on a substrate (esp. for elec. circuit connections) is precoated with a thin layer of low-m.p. solder alloy for surface protection, and then is impacted with a molten microdroplet of higher-m.p. solder alloy to form a **solder bump** by spreading. The microdroplet is typically formed of a molten **Sn-Pb** solder with the m.p. >160.degree., and is impacted on the **Sn-Bi** or In alloy solder layer having the m.p. <160.degree., resulting in the surface melting and bump formation to cover the **Cu pad** surface. The microdroplet size is typically 25-50 .mu.m. vs. the initial solder-layer thickness of <50 .mu.m. The solder-coated **Cu pad** is optionally impacted with sequential microdroplets to build up the solder layer by fusion contact and consistent alloying. The resulting **solder bumps** are suitable for elec. connections on **integrated circuits**.

L75 ANSWER 40 OF 47 HCAPLUS COPYRIGHT 2003 ACS
AN 1996:677570 HCAPLUS
DN 125:313672
TI FCOB reliability evaluation simulating multiple rework/reflow processes
AU Chen, Wayne; Gentile, John; Higgins, Leo
CS Motorola, Austin, TX, 78762, USA
SO Proceedings - Electronic Components & Technology Conference (1996), 46th, 1184-1195
CODEN: PETCES
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
AB Flip **chip** assembly (Direct **Chip** Attach (DCA), or Flip **Chip** on Board (FCOB)) on Printed Wiring Boards, in conjunction with conventional leaded device surface mount technol., is beginning to proliferate in compact and portable systems. DCA with conventional C4 bumps requires solder coated bond pads to allow joining in typical SMT reflow cycles. A flip **chip** device on a typical FCOB/SMT board will usually experience no high temp. excursions after the **die** joining and underfill encapsulant cure unless the board undergoes a rework cycle. FCOB single **chip** packages and multichip modules are now in development with std. C4 bumps, and a new Motorola "E-3" bump which requires no solder on bond pads. These solder interconnects must be stable through multiple heat treatments expected in subsequent system level assembly and repair operations. Flip **Chip** Plastic **Ball Grid** Arrays (FC-PBGAs) will typically undergo three solder reflow, or reheat, cycles to .apprx.220.degree.C subsequent to initial flip **chip** reflow assembly. The multiple reheats are for **BGA** ball attach, board level **BGA** SMT assembly, second

side **BGA** SMT assembly, and possible rework operations. In this paper, the effect of multiple reheats on the solder connection microstructure and strength (before, and after, underfill encapsulation), and the integrity of the underfill encapsulant adhesive and cohesive strength is reported, using both FCOB single **chip** packages and multiple **chip** modules. The effect of multiple reheats on elec. resistance of daisy chain nets, and **die** stress (radius of curvature), is also reported. Hot air gun rework (before underfill) is simulated and std. belt furnace reflows are utilized. Cross-sections of bump connections and underfill interfaces were studied to assess changes induced by the temp. exposures. The reliability of the FCOB assemblies was assessed via temp. cycle, thermal shock and autoclave tests.

L75 ANSWER 41 OF 47 HCAPLUS COPYRIGHT 2003 ACS
AN 1995:280432 HCAPLUS
DN 122:120277
TI A flip **chip** process based on electroplated **solder bumps**
AU Salonen, J.; Salmi, J.
CS VTT Electronics, EMC, Espoo, FIN-02150, Finland
SO Physica Scripta, T (1994), T54(Proceedings of 16th Nordic Semiconductor Meeting, 1994), 230-3
CODEN: PHSTER; ISSN: 0281-1847
PB Royal Swedish Academy of Sciences
DT Journal
LA English
AB Sputter deposited Mo and Cu were used as thin film layers between the Al pads and the **solder bumps**. A reason for this choice is that the metals can be selectively etched after bumping using the bumps as a mask, thus circumventing the need for a sep. mask for etching the thin film metals. The bumps are electroplated from a binary **Pb-Sn** bath using a thick liq. photoresist. An extensively modified com. flip **chip** bonder was used for alignment and bonding. Heat assisted tack bonding was used to attach the **chips** to the substrate, and final reflow joining is done without flux in a vacuum furnace.

L75 ANSWER 42 OF 47 HCAPLUS COPYRIGHT 2003 ACS
AN 1994:713575 HCAPLUS
DN 121:313575
TI **Solder bump** terminals for mounting **integrated circuit chips**
PA International Business Machines Corp., USA
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 06112213	A2	19940422	JP 1993-154683	19930625
PRAI US 1992-938074		19920831		

AB Metal layers (e.g., Cr and Cu) formed on substrates across passivation films are etched with **solder bump** terminals as masks to create stepped edge profiles. The passivation films are less likely to have cracks.

L75 ANSWER 43 OF 47 HCAPLUS COPYRIGHT 2003 ACS
AN 1992:179015 HCAPLUS
DN 116:179015
TI Investigations of laser soldered TAB inner lead contacts

AU Zakel, E.; Azdasht, G.; Reichl, H.
CS Tech. Univ. Berlin, Berlin, Germany
SO Hybrid Circuits (1992), 27, 7-13
CODEN: HYCRD5; ISSN: 0265-3028
DT Journal
LA English
AB The results of tape automated bonding (TAB) inner lead with a pulsed Nd:YAG laser are presented. Tapes with three metalizations (**Sn**, Ni-**Sn** and Au) were laser soldered to bumps consisting of Au and Au-**Sn**. The pull strength of laser soldered TAB contacts was optimized by variation of laser power, and reliability investigations were performed. The metallurgy of laser soldering is different and more crit. to long-term reliability than that of gang bonded contacts, even if identical tape and bump metals are used. An accumulation of eutectic 80/20 Au-**Sn** solder in the bonded interface results in degrdn. due to Kirkendall pore formation in the Cu-**Sn**-Au system. Application of a tape with a diffusion barrier of Ni inhibits this effect. During thermal aging, these contacts show degrdn. of pull forces which is attributed to formation of brittle intermetallic compds. of Ni, **Sn** and Au in the contact area. Laser soldering of Au-plated tapes to Au-**Sn solder bumps** is possible. The contacts show optimum pull forces and min. degrdn. after thermal aging. This behavior is attributed to the formation of an intermetallic compd. having a high stability. The zeta phase acts as a diffusion barrier between the Cu lead and eutectic Au-**Sn** solder.

L75 ANSWER 44 OF 47 HCAPLUS COPYRIGHT 2003 ACS
AN 1991:148300 HCAPLUS
DN 114:148300
TI Flip-**chip** soldering to bare copper circuits
AU Ingraham, Anthony P.; McCreary, jack M.; Varcoe, Jack A.
CS Technol. Lab., IBM Corp., Endicott, NY, 13760, USA
SO IEEE Transactions on Components, Hybrids, and Manufacturing Technology (1990), 13(4), 656-60
CODEN: ITTEDR; ISSN: 0148-6411
DT Journal
LA English
AB Controlled collapse **chip** connection C4 technol. was introduced as a **chip** interconnection. A process for providing high yield/high reliability C4 joining to bare Cu circuitry is described. A study was undertaken in the course of implementing a major change in metalized ceramic and metalized ceramic polyimide prodn. line. The study involved joining **chips** with 95/5 **Pb**/**Sn** C4 **solder bumps** to bare **Cu pads** on substrates to replace dip tinned substrates with 90/10 **Pb**/**Sn** coated pads. Included is an extensive anal. of the C4 interconnection. Over 30,000 **chips** were joined to ceramic substrates to characterize wetting of the **Cu pads**, evaluate C4 fatigue life, and asses any reliability impact of natural and artificially induced defects in the C4 columns or wetted pad surface. The technique for C4 interconnection joining to **Cu pads** was successfully implemented across many manufg. sites.

L75 ANSWER 45 OF 47 HCAPLUS COPYRIGHT 2003 ACS
AN 1985:440977 HCAPLUS
DN 103:40977
TI Study of the **tin-copper metallurgical** reaction at **solder bumps**
AU Tsutsumi, Kazuhito; Kohara, Masanobu; Shibata, Hiroshi; Nakata, Hidefumi
CS LSI Res. Dev. Lab., Mitsubishi Electr. Corp., Itami, 664, Japan
SO International Journal for Hybrid Microelectronics (1984), 7(4), 38-43

CODEN: IMICDJ; ISSN: 0277-8270
DT Journal
LA English
AB Intermediate layers of Cr/Cu/Au were prepd. on an Al **chip** pad by continuous deposition and placed between the pad and **Pb**-5% **Sn** [39315-20-3] **solder ball**. Elec. resistance of the **solder-ball** structure at every step in its construction, internal bend stress in the intermediate layer, and nominal breaking stress of the joint were measured as a function of the Cu layer thickness. Atoms in the Cu layer are consumed by formation of Cu-**Sn** intermetallic compds. (Cu6Sn5 [12019-69-1], Cu3Sn [12019-61-3]) in the solder during the metallurgical reaction which occurs during the solder reflow. The compds. are brought into contact with the Cu layer under the Cu layer and decrease the ohmic contact area and nominal breaking stress of the joint. SEM observations of the cleaned faces after measurement of the breaking stress were made. When the Cu layer is .gtoreq.2 .mu. thick and subjected to heat treatment at a relatively low temp. prior to soldering, the layer of dissoln. products formed in the solder reflow process does not reach the layer of dissoln. products and results in a high strength joint.

L75 ANSWER 46 OF 47 HCAPLUS COPYRIGHT 2003 ACS
AN 1976:596910 HCAPLUS
DN 85:196910
TI Microspheres of solder material with a metallic core
IN Takahashi, Eikichi; Taguchi, Toshihiko; Fujikura, Kazuo; Sudo, Toshihisa
PA Senju Metal Industry Co., Ltd., Japan
SO Ger. Offen., 17 pp.
CODEN: GWXXBX
DT Patent
LA German
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	DE 2601765	A1	19760729	DE 1976-2601765	19760119
	JP 51086043	A2	19760728	JP 1975-10223	19750124
	JP 55035238	B4	19800912		
	GB 1476599	A	19770616	GB 1975-53034	19751229
	US 4097266	A	19780627	US 1975-645395	19751230
PRAI	JP 1975-10223		19750124		

AB Microspherical soldering composites having a spherical metal core made from an elec. conductive and wettable **metal**, such as **Cu**, Ag or their alloys, and a >20.mu. thick coating of a soldering compn., for example **Sn**, **Pb**, Ag and their alloys, are made for soldering contacts to integrated elec. circuits. The microspheres are made by heating in a suitable app. spherical Ag cores of 0.25 mm diam. in the presence of a **Sn**-40%**Pb** [11137-19-2] **solder sphere** of approx. same size and a flux. The temp. used for coating is greater than the m.p. of the solder, but less than the m.p. of the core.

L75 ANSWER 47 OF 47 HCAPLUS COPYRIGHT 2003 ACS
AN 1974:418371 HCAPLUS
DN 81:18371
TI Making contact bumps on flip-**chips**
IN Brown, Ronald E.; Oakes, James A.
PA General Motors Corp.
SO U.S., 6 pp.
CODEN: USXXAM
DT Patent
LA English

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 3809625	A	19740507	US 1972-280795	19720815
PRAI	US 1972-280795		19720815		

AB A semiconductor **wafer** contg. .gtoreq.1 active device is coated with an oxide contg. windows. An Al metallization pattern is formed and, over it, a continuous glass film is formed with holes over the regions intended for contact pads. A continuous layer of Cr is deposited. Contact pads, e.g. of Au, are formed on the Cr over the holes in the glass. The pads on the unmasked **wafer** are plated selectively, e.g. with Ag, which does not deposit on Cr. The Ag bumps are plated with Au and the exposed Cr is removed by etching. The glass layer protects the device from contamination. Alternatively, contact **pads** of **Cu-Sn** double layers and bumps of a **Pb**-10 wt.% **Sn** solder alloy may be formed in combination. The **solder bumps** are subjected to reflowing.

L84 ANSWER 1 OF 39 HCAPLUS COPYRIGHT 2003 ACS
AN 2003:97923 HCAPLUS
DN 138:119581
TI Guided mode resonant filter biosensor using a linear grating surface structure
IN Cunningham, Brian T.; Pepper, Jane; Lin, Bo; Li, Peter; Qiu, Jean; Pien, Homer
PA SRU Biosystems, LLC, USA
SO U.S. Pat. Appl. Publ., 91 pp., Cont.-in-part of U.S. 2002 127,565.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 11

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2003027328	A1	20030206	US 2002-59060	20020128
	US 2002127565	A1	20020912	US 2001-930352	20010815
	US 2003032039	A1	20030213	US 2002-180647	20020626
	US 2003059855	A1	20030327	US 2002-180374	20020626
	US 2003017580	A1	20030123	US 2002-196058	20020715
	US 2003017581	A1	20030123	US 2002-201818	20020723
	US 2003026891	A1	20030206	US 2002-201878	20020723
	US 2003068657	A1	20030410	US 2002-237641	20020909
	US 2003077660	A1	20030424	US 2002-253846	20020925
PRAI	US 2000-244312P	P	20001030		
	US 2001-283314P	P	20010412		
	US 2001-303028P	P	20010703		
	US 2001-930352	A2	20010815		
	JP 2001-299942	A	20010928		
	US 2002-52626	A2	20020117		
	US 2002-58626	A2	20020128		
	US 2002-59060	A2	20020128		
	US 2002-180374	A2	20020626		
	US 2002-180647	A2	20020626		
	US 2002-196058	A2	20020715		
	US 2002-227908	A2	20020826		

AB Methods and compns. are provided for detecting biomol. interactions. The use of labels is not required and the methods can be performed in a high-throughput manner. The invention also provides optical devices useful as narrow band filters.

L84 ANSWER 2 OF 39 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:734127 HCAPLUS
DN 137:270533
TI Fabrication of multilayer wiring semiconductor devices containing a heat-resistant polybenzoxazole protective film
IN Kenmochi, Tomoki; Hirano, Takashi
PA Sumitomo Bakelite Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2002278090	A2	20020927	JP 2001-78378	20010319
PRAI	JP 2001-78378		20010319		

OS MARPAT 137:270533
AB The title semiconductor devices are fabricated by steps of: forming a heat-resistant photosensitive polybenzoxazole (or polyimide) protective

film (A) on a silicon **wafer**, exposing A under a light source to form pattern, applying a metal layer (B) on A such as by **sputtering**, coating a pos. photoresist (C), e.g., AZ 1500, on B, patterning C by exposing under a light source, **etching** B with acid soln., and finally peeling off C using a liq. contg. polyoxyalkylenes and alkanolamines, e.g., dipropylene **glycol** monomethyl ether and isopropanolamine, wherein B is selected from aluminum and copper.

L84 ANSWER 3 OF 39 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:582796 HCAPLUS
DN 137:239617
TI Three-dimensional pattern transfer and nanolithography: modified soft molding
AU Kim, Y. S.; Park, Joonhyung; Lee, Hong H.
CS School of Chemical Engineering, Nanoelectronics Institute Seoul National University, Seoul, 151-744, S. Korea
SO Applied Physics Letters (2002), 81(6), 1011-1013
CODEN: APPLAB; ISSN: 0003-6951
PB American Institute of Physics
DT Journal
LA English
AB One-step transfer of molded three-dimensional polymer structures into underlying substrate is reported. The one-step transfer is made possible by a molding technique presented here in the form of modified soft molding. Formation of a desired three-dimensional structure in a polymer film by this method, followed by one-step reactive ion **etching**, is utilized for the transfer. The technique is also shown to be effective in transferring sub-100-nm features.
RE.CNT 9 THERE ARE 9 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L84 ANSWER 4 OF 39 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:540238 HCAPLUS
DN 137:102484
TI Chemically enhanced focused ion-beam micromachining of copper on substrate
IN Russell, Phillip E.; Griffis, Dieter P.; Perez, Juan Carlos Gonzales
PA USA
SO U.S. Pat. Appl. Publ., 14 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002094694	A1	20020718	US 2001-871541	20010531
	US 6514866	B2	20030204		
	US 2003060048	A1	20030327	US 2002-284784	20021031
PRAI	US 2001-261109P	P	20010112		
	US 2001-871541	A3	20010531		

AB A method of micromachining a copper layer on a substrate, e.g., **microelectronic** substrate, is carried out by maintaining the substrate in a vacuum, bombarding a portion of the substrate with a focused particle beam from a particle source, and exposing the substrate to a supply of org. chloride or org. hydroxide during particle bombardment. The org. chloride or org. hydroxide concn. at the substrate is an amt. sufficient to enhance the relative removal of the copper layer by decreasing the removal of the dielec. or increasing the removal of the copper or a combination of both.

L84 ANSWER 5 OF 39 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:315255 HCAPLUS

DN 136:302864
TI Post-**etching** cleaning of a copper-associated dielectric
IN Lallier, Jean-Pierre
PA Atofina, Fr.
SO PCT Int. Appl., 8 pp.
CODEN: PIXXD2
DT Patent
LA French
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 2002033742	A1	20020425	WO 2001-FR3141	20011011
	W: CA, CN, IL, JP, KR, MX, PL, SG, US				
	RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR				
	FR 2815359	A1	20020419	FR 2000-13267	20001017
PRAI	FR 2000-13267	A	20001017		

AB In order to eliminate residues after **etching** a copper-assocd. dielec., the method consists in using a cleaning compn. consisting, by wt., of: 35 to 85 % of dimethylsulfoxide or N-methylpyrrolidone, 11 to 49 % of 3-methoxypropylamine, 0 to 8 % of water, and 0 to 10 % of at least a corrosion inhibitor such as catechol.
RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L84 ANSWER 6 OF 39 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:312982 HCAPLUS
DN 136:302810
TI Procedure for the preparation of a capacitor with deep trenches for the structural analysis and associated structural analysis procedure
IN Lee, Thing-Jong
PA Promos Technologies, Inc., Taiwan; Mosel Vitelic Inc.; Infineon Technologies Ag
SO Ger. Offen., 10 pp.
CODEN: GWXXBX
DT Patent
LA German
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	DE 10050049	A1	20020425	DE 2000-10050049	20001010
	US 6403439	B1	20020611	US 2000-629733	20000731
PRAI	DE 2000-10050049	A	20001010		

AB A procedure is presented for the prepn. of a capacitor with deep trenches for structural anal. using a combination of mech. and chem. effects to expose the trench capacitors. The procedure for the prepn. this comprises the following steps: (A) mech. treating of the back of the **dies** to remove a 1st section of the substrate and leave and a 2nd section of the substrate intact; (B) installing the mech. treated **dies** with its top side facing an assembly fixture; and (C) chem. treating the mounted **dies** to remove the 2nd section of the substrate and expose a chem. treated **die**. By exposing the capacitors with deep trenches, the procedure facilitates the study of the equipment for examg. possible structural defects, e.g., metallic short circuits, condenser holes, and particle defects. The procedure overcomes the difficulties that arise with conventional procedures for removing a substrate and facilitates the study by different procedures. The procedure facilitates, e.g., the elucidation of As glass remnants, and of deformations of deep trenches that arise through the length of the deep trench and within the thickness of the oxide-nitride layer of the deep trench.

RE.CNT 2 THERE ARE 2 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L84 ANSWER 7 OF 39 HCAPLUS COPYRIGHT 2003 ACS
AN 2001:145246 HCAPLUS
DN 134:171970
TI Low temperature rinse of **etching** agents in device fabrication
IN Gilton, Terry L.
PA Micron Technology, Inc., USA
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6194326	B1	20010227	US 2000-544721	20000406
PRAI US 2000-544721		20000406		

AB A **wafer** cleaning process is disclosed for quenching **etch** reactions while rinsing **etch** reactants and **etch** products from the **wafer**. Holes are **etched** through an insulating layer by reactive ion **etch**, for example. The holes might comprise contact openings over a semiconductor substrate, or vias through insulating layers between metal lines. An org. or polymer residue left in the holes is cleaned by a wet process. The cleaning process continues to attack sidewalls of the holes, undesirably widening them. The **wafer** is therefore rinsed with a rinse agent <0.degree., thermally quenching further **etching** of the sidewalls and affording greater control over the hole dimensions. At the same time, the rinse agent allows relatively rapid diffusion of etchants and **etch** products from narrow and deep openings. An exemplary rinse agent for such low temp. rinsing is dil. ethylene **glycol**.

RE.CNT 5 THERE ARE 5 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L84 ANSWER 8 OF 39 HCAPLUS COPYRIGHT 2003 ACS
AN 2000:496844 HCAPLUS
DN 133:303169
TI Fabrication of gratings and design of diffractive optical elements embossed on sol-gel films
AU Tan, Gu; Chan, Yuen Chuen; Liu, Jian; Liaw, ChinYi; Lam, Yee-Loy; Zhou, Yan
CS School of EEE, Photonics Research Group, Nanyang Technological Univ., Singapore, Singapore
SO Proceedings of SPIE-The International Society for Optical Engineering (1999), 3896(Design, Fabrication, and Characterization of Photonic Devices), 412-416
CODEN: PSISDG; ISSN: 0277-786X
PB SPIE-The International Society for Optical Engineering
DT Journal
LA English
AB Ion exchange, plasma deposition and flame hydrolysis are typically employed techniques for fabricating glass waveguides and gratings. These techniques have several drawbacks such as involvement of expensive instruments, multi-step procedure and high temp. treatment. These drawbacks make it difficult for their adoption mass prodn. The sol-gel process is a simple and inexpensive way for making glass, and embossing into sol-gel films provides a simple alternative for fabricating surface profile gratings and other integrated optical devices. The authors report the usage of the embossing technique to fabricate gratings and diffractive optical elements (DOEs) in the sol-gel cladding layer of a waveguide. The

designed DOEs manipulate out-coupled light from a slab waveguide and form 3 lines of equal intensity at a stipulated distance. The DOEs were designed as two-level optics by the direct binary search method based on the scalar diffractive theory, and the master molders used in the embossing were fabricated by UV laser writing on photoresist combined with reactive ion **etching**. The authors chose org. modified silane in the sol-gel process and no baking was needed, greatly minimizing possible shrinkage of the thin film.

RE.CNT 9 THERE ARE 9 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L84 ANSWER 9 OF 39 HCAPLUS COPYRIGHT 2003 ACS
AN 2000:297914 HCAPLUS
DN 133:44481
TI Intelligent biomembrane obtained by irradiation techniques
AU Kaetsu, Isao; Uchida, Kumao; Sutani, Kouichi; Sakata, Shoei
CS Department of Nuclear Engineering, Faculty of Science and Technology, Kinki University, Osaka, 577-8502, Japan
SO Radiation Physics and Chemistry (2000), 57(3-6), 465-469
CODEN: RPCHDM; ISSN: 0969-806X
PB Elsevier Science Ltd.
DT Journal
LA English
AB An intelligent biomembrane for environment-responsive feedback releases has been developed using radiation techniques. Various fine-porous base membranes (polyester, polycarbonate, silicon) were prepd. by hole fabrication techniques with excimer-laser, ion-beam **etching** and photo-lithog. **etching**. Then, various monomeric mixt. of stimuli-sensitive hydrogels with or without immobilized enzymes were coated and polymd. on the porous membrane by UV, .gamma.-ray or electron beam. The product showed the intelligent feedback release functions of model substance (methylene blue) in response to the on-off switching of signals such as pH changes and introduction of elec. field. The responsiveness was remarkably improved by radiation induced IPN (interpenetrating polymer network) formation. Intelligent release controlled by a computer program was also studied and proved.

RE.CNT 5 THERE ARE 5 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L84 ANSWER 10 OF 39 HCAPLUS COPYRIGHT 2003 ACS
AN 2000:157691 HCAPLUS
DN 132:201831
TI Process for removing **etching** residues, **etching** mask, and silicon nitride and/or silicon dioxide
IN Rath, David L.; Jagannathan, Rangarajan; McCullough, Kenneth J.; Okorn-Schmidt, Harald F.; Madden, Karen P.; Pope, Keith R.
PA International Business Machines Corporation, USA
SO U.S., 4 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6033996	A	20000307	US 1997-969595	19971113
	TW 387096	B	20000411	TW 1998-87109099	19980608
PRAI	US 1997-969595	A	19971113		

AB **Etching** residue, **etching** mask, and Si nitride and/or SiO2 are **etched** or removed by using a compn. contg. a fluoride-contg. compd., H2O, and certain org. solvents.

RE.CNT 52 THERE ARE 52 CITED REFERENCES AVAILABLE FOR THIS RECORD

ALL CITATIONS AVAILABLE IN THE RE FORMAT

L84 ANSWER 11 OF 39 HCAPLUS COPYRIGHT 2003 ACS
AN 2000:98180 HCAPLUS
DN 132:145388
TI Dry-**etching** method and apparatus, a photomask and its preparation, and a semiconductor circuit and its fabrication
IN Sasaki, Takaei; Harashima, Noriyuki; Aoyama, Satoshi; Sakamoto, Shouichi
PA Ulvac Coating Corporation, Japan; Mitsubishi Denki Kabushiki Kaisha
SO Eur. Pat. Appl., 27 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 978870	A2	20000209	EP 1999-115511	19990805
	EP 978870	A3	20000524		
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	JP 2000114246	A2	20000421	JP 1998-309002	19981029
	US 6391791	B1	20020521	US 1999-361159	19990727
	KR 2000017156	A	20000325	KR 1999-32354	19990806
	TW 393591	B	20000611	TW 1999-88113479	19990806
	US 2002136967	A1	20020926	US 2002-107439	20020328
	US 2002139476	A1	20021003	US 2002-107329	20020328
	US 2002155723	A1	20021024	US 2002-107322	20020328
PRAI	JP 1998-224845	A	19980807		
	JP 1998-309002	A	19981029		
	US 1999-361159	A3	19990727		

AB A method for dry **etching** a metal film uses, as an **etching** gas, a mixed gas including (a) a reactive ion **etching** gas which contains an O-contg. gas and a halogen-contg. gas, and (b) a reducing gas. The dry-**etching** method permits the prodn. of a photomask by forming patterns to be transferred to a **wafer** on a photomask blank. The photomask can in turn be used for manufg. semiconductor circuits. The method permits the decrease of the dimensional difference due to the coexistence of coarse and dense patterns in a plane and the prodn. of a high-precision pattern-**etched** product.

L84 ANSWER 12 OF 39 HCAPLUS COPYRIGHT 2003 ACS
AN 1999:686665 HCAPLUS
DN 131:294327
TI Photolithography alignment mark manufacturing process in tungsten CMP metallization for **integrated circuits**
IN Tseng, Horng-Huei
PA Vanguard International Semiconductor Corporation, Taiwan
SO U.S., 12 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5972793	A	19991026	US 1997-868844	19970609
	US 6080636	A	20000627	US 1999-379280	19990823
PRAI	US 1997-868844	A3	19970609		

AB A method is disclosed for forming alignment marks at the outer perimeter of **wafers** where they are not susceptible to much damage during chem.-mech. polishing (CMP) process. Complete protection is provided by

recessing the alignment mark into the substrate by **etching**. Recess **etching** is accomplished at the same time the isolation trenches are formed to delineate device areas. Thus, alignment marks are provided with a protective recess without extra steps. Also, by forming alignment marks at the outer perimeter of the **wafer**, productivity is improved by providing max. usage of **wafer** area for **integrated circuits**.

RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L84 ANSWER 13 OF 39 HCAPLUS COPYRIGHT 2003 ACS
AN 1999:566283 HCAPLUS
DN 131:178564
TI Cooling system with antifreeze for cooling rotating magnetron for process chamber of vacuum processing system in fabrication of **integrated circuits** and flat-panel displays
IN Fu, Jianming; Sinha, Ashok K.
PA Applied Materials, Inc., USA
SO PCT Int. Appl., 23 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 9944220	A1	19990902	WO 1999-US3680	19990219
	W: JP, KR				
	RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
	EP 1058944	A1	20001213	EP 1999-908293	19990219
	R: BE, DE, GB, NL				
	JP 2002505504	T2	20020219	JP 2000-533889	19990219
	TW 432118	B	20010501	TW 1999-88102795	19990317
PRAI	US 1998-30264	A	19980225		
	WO 1999-US3680	W	19990219		

AB A vacuum processing system has a process chamber with a rotating member, such as a magnetron in a **PVD** chamber, disposed in a cooling chamber contg. a free O deficient cooling fluid that circulates into and out of the cooling chamber. The free O deficient cooling fluid may be an ethylene-**glycol** based coolant or antifreeze. Conduits connect an inlet and an outlet of the cooling chamber to a heat exchanger to cool and re-circulate the free O deficient cooling fluid.

RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L84 ANSWER 14 OF 39 HCAPLUS COPYRIGHT 2003 ACS
AN 1999:329973 HCAPLUS
DN 130:331326
TI Cleaning step which improves electromigration performance of interlayer connection in **integrated circuits**
IN Brumley, Mark D.
PA Intel Corporation, USA
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5904560	A	19990518	US 1996-623672	19960329
PRAI	US 1996-623672		19960329		

AB An improved cleaning step for cleaning interconnects such as W filed vias or contacts. After the W plugs were formed substantially coplanar with the surrounding dielec. surface (or adhesion or barrier layer surface), the **wafers** are cleaned in a sequence of chems. that finishes in a soln. that includes H2O2. The temp. and concns. of the active agents are chosen such that **etching** is minimized until the application of sonic energy. This light **etching** of the interconnect W and cleaning of the exposed surface was found to better prep. these surfaces for receiving an overlying metal layer. The electromigration performance of the overlying metal layer shows substantial improvement when this cleaning step was used. The cleaning step was used following an ethylene **glycol**-HF mixt. cleaning step, dependent on the degree of interconnect and dielec. coplanarity after the W **etch** step. The prior art step of Ar **sputtering** is not needed to obtain the improved electromigration performance. Device yields may be substantially improved depending on the level of **wafer** cleanliness prior to the application of the clean.

RE.CNT 5 THERE ARE 5 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L84 ANSWER 15 OF 39 HCAPLUS COPYRIGHT 2003 ACS
AN 1999:212658 HCAPLUS
DN 130:216832
TI Forming a via through a **microelectronics** layer susceptible to **etching** by a fluorine-containing plasma followed by an oxygen-containing plasma
IN Yu, Chen-hua
PA Taiwan Semiconductor Manufacturing Company, Ltd., Taiwan
SO U.S., 16 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 5888309	A	19990330	US 1997-998635	19971229
PRAI US 1997-998635		19971229		

AB There is 1st provided a substrate employed in fabrication of **microelectronic** devices, including **integrated circuits**, solar cells, ceramic substrates, and flat-panel displays. There is then formed over the substrate a **microelectronics** layer formed of a material susceptible to sequential **etching** employing a F-contg. plasma followed by an O-contg. plasma. A patterned photoresist layer is then formed on the **microelectronics** layer. The **microelectronics** layer is then **etched** through use of the F-contg. plasma using the patterned photoresist layer as a mask to form a patterned **microelectronics** layer having a via formed through it. The F-contg. plasma **etch** method simultaneously forms a fluorocarbon polymer residue layer on a sidewall of the via. The patterned photoresist layer is then stripped through use of the O-contg. plasma from the patterned **microelectronics** layer while leaving a no greater than partially **etched** fluorocarbon polymer residue on the sidewall of the via. Finally, the fluorocarbon polymer residue is stripped from the sidewall of the via through use of a wet chem. stripping method.

RE.CNT 9 THERE ARE 9 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L84 ANSWER 16 OF 39 HCAPLUS COPYRIGHT 2003 ACS
AN 1999:99340 HCAPLUS
DN 130:229697

TI Development of the SC-RTA process for fabrication of sol-gel based silica-on-silicon integrated optic components
AU Syms, R. R. A.; Holmes, A. S.; Huang, W.; Schneider, V. M.; Green, M.
CS Optical and Semiconductor Devices Section, Dept. of Electrical and Electronic Engineering, Imperial College, London, SW7 2BT, UK
SO Journal of Sol-Gel Science and Technology (1998), 13(1/2/3), 509-516
CODEN: JSGTEC; ISSN: 0928-0707
PB Kluwer Academic Publishers
DT Journal
LA English
AB The SC-RTA (spin coating - rapid thermal annealing) process for fabricating silica-on-silicon planar lightwave circuits from sol-gel glass is described. A wide range of glasses was deposited, process temps. were reduced, and components fabricated by reactive ion **etching**, reflow and burial of channel guides showed steadily decreasing loss. Propagation losses are .apprxeq.0.2 dB/cm at .lambda. = 1.523 .mu.m in a high .DELTA.n system. Passive components demonstrated include tree-structured power splitters and thermo-optic switches.
RE.CNT 20 THERE ARE 20 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L84 ANSWER 17 OF 39 HCAPLUS COPYRIGHT 2003 ACS
AN 1999:90279 HCAPLUS
DN 130:132789
TI Selective partial curing of spin-on-glass by ultraviolet radiation to protect **integrated circuit dice** near the **wafer** edge
IN Tsai, Chia-shiung; Tseng, Pin-nan; Hsu, Sung-mu
PA Taiwan Semiconductor Manufacturing Company Ltd., Taiwan
SO U.S., 6 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5866481	A	19990202	US 1996-660305	19960607
PRAI	US 1996-660305		19960607		

AB This invention relates to a method for protecting regions of a spin-on-glass(SOG) layer, which covers usable semiconductor **dice**, from dissoln. damage during an **etch** step which removes SOG along the **wafer** edge. The endangered **dice** have portions which lie in the area affected by the edge rinse. Instead of performing the edge **etching** step immediately after the deposition of the SOG, the endangered **dice** are 1st selectively partially cured by exposure to UV radiation. This makes the SOG over these **dice** resistant to the SOG solvent used for the edge rinse. Up to ten percent of the total usable **dice** on the **wafer** can be salvaged by the method of this invention.
RE.CNT 11 THERE ARE 11 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L84 ANSWER 18 OF 39 HCAPLUS COPYRIGHT 2003 ACS
AN 1999:21615 HCAPLUS
DN 130:87970
TI Method for producing a micro optical semiconductor lens
IN Tran, Dean; Anderson, Eric R.; Strijek, Ronald L.; Rezek, Edward A.
PA TRW Inc., USA
SO U.S., 13 pp.
CODEN: USXXAM
DT Patent

LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5853960	A	19981229	US 1998-40636	19980318
	JP 11298046	A2	19991029	JP 1998-372169	19981228
PRAI	US 1998-40636		19980318		

AB Methods for fabricating Group III-V semiconductor microlenses for hybrid integration with microoptical devices are described which entail forming lenses from a semiconductor **wafer** by selectively **etching** a surface of the semiconductor **wafer** and forming a lens arm from the semiconductor **wafer** on a surface opposite the surface by selectively **etching** the surface of the semiconductor **wafer**. The lens and lens arm may then be cleaved from the substrate **wafer** and directly mounted to a microoptical device. The lens may be provided with an antireflective coating and the lens arm may be metalized prior to cleaving. The **etching** step may be a wet or dry **etch**. By using a semiconductor material to form the lenses the thermal stability of the integrated systems is enhanced over conventional systems.

RE.CNT 12 THERE ARE 12 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L84 ANSWER 19 OF 39 HCAPLUS COPYRIGHT 2003 ACS
AN 1998:282379 HCAPLUS
DN 128:329869
TI Technique for the removal of residual spin-on-glass (SOG) after full SOG etchback
IN Wu, Lin-june; Yu, Chen-hua Douglas; Lee, Jin-yuan
PA Taiwan Semiconductor Manufacturing Company, Ltd., Taiwan
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5747381	A	19980505	US 1996-599770	19960212
PRAI	US 1996-599770		19960212		

AB This invention relates to a method for removing residual spin-on-glass (SOG) during a planarization processing step wherein the SOG is used as a sacrificial planarization medium and subjected to a full etchback to an underlying interlevel dielec. (ILD) layer. The SOG is applied over the ILD layer, and **etched** back into the ILD layer by reactive-ion-**etching** under conditions of comparable **etch** rates for both SOG and ILD. At endpoint there some residual pockets of SOG can be present as well as a region of SOG along the edges of the **wafer** where it is clamped in the etchback tool. The residual SOG must be removed completely to avoid SOG cracking after thermal processing and SOG outgassing during subsequent metal deposition. For this purpose an aq. **etch** consisting of hydrofluoric acid buffered with ammonium fluoride is used. The **etchant** compn. chosen exhibits a selectivity for SOG over the ILD glass of greater than 40 making it suitable for removing considerable SOG residues with minimal attack of the ILD.

RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L84 ANSWER 20 OF 39 HCAPLUS COPYRIGHT 2003 ACS
AN 1997:102993 HCAPLUS
DN 126:193603

TI Plasma charging induced gate oxide damage during metal **etching** and ashing
AU Lin, H. C.; Perng, C. H.; Chien, C. H.; Chiou, S. G.; Chang, T. F.; Huang, T. Y.; Chang, C. Y.
CS National Nano Device Laboratory, National Chiao-Tung University, Taiwan
SO International Symposium on Plasma Process-Induced Damage, 1st, Santa Clara, Calif., May 13-14, 1996 (1996), 113-116. Editor(s): Cheung, Kin P.; Nakamura, Moritaka; Gabriel, Calvin T. Publisher: Northern California Chapter of the American Vacuum Society, Sunnyvale, Calif.
CODEN: 63YRAU
DT Conference
LA English
AB Gate oxide damage induced by plasma charging during metal **etching** with magnetically enhanced reactive ion **etching** (MERIE) or helicon wave **etcher** and subsequent resist ashing was investigated. It was found that serious damage would occur during the MERIE processing, while good results were obtained with helicon wave **etcher**. It was also obsd. that the antenna effect can be clearly illustrated by measuring the gate current.

L84 ANSWER 21 OF 39 HCAPLUS COPYRIGHT 2003 ACS
AN 1996:722539 HCAPLUS
DN 126:25641
TI Making an aluminum-containing interconnect without hardening a sidewall protection layer
IN Yachi, Masaharu
PA Seiko Epson Corporation, Japan
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5578163	A	19961126	US 1992-962818	19921019
PRAI	JP 1991-272760		19911021		
	JP 1991-279114		19911025		
	JP 1992-293892		19921006		

AB A method for manufg. a semiconductor device includes (a) dry-**etching** an Al-contg. interconnecting layer, which is formed on a **wafer**, using a reactive gas contg. Cl and/or chloride; (b) converting a reactive gas which contains a compd. having .gtoreq.1 H atom into a plasma at 20-150.degree. and removing the remaining Cl by activated H; and (c) converting an O-contg. reactive gas into a plasma at 20-150.degree. and removing a resist layer chiefly by ashing. If the temps. in the steps (b) and (c) are set low, there is no obstacle to removing a sidewall protection layer formed by **etching** the Al-contg. interconnecting layer.

L84 ANSWER 22 OF 39 HCAPLUS COPYRIGHT 2003 ACS
AN 1996:644802 HCAPLUS
DN 126:52719
TI Wet silylation and oxygen plasma development of photoresists: A mature and versatile lithographic process for **microelectronics** and microfabrication
AU Gogolides, Evangelos; Tzevelekis, Dimitrios; Grigoropoulos, Spyridon; Tegou, Evangelia; Hatzakis, Michael
CS Inst. Microelectronics, NCSR Demokritos, 15310, Greece
SO Journal of Vacuum Science & Technology, B: Microelectronics and Nanometer Structures (1996), 14(5), 3332-3338
CODEN: JVTBD9; ISSN: 0734-211X

PB American Institute of Physics
DT Journal
LA English
AB A near-surface imaging process using wet silylation and oxygen plasma development is described. New characterization techniques of films spun on **wafers** are presented for: (a) quant. Si concn. detn. using proton NMR spectroscopy (H), and (b) glass transition and/or flow temp. detn. (Tg) of the silylated photoresist using thermomech. anal. H-line, I-line, and deep-UV lithog. (at 248 nm) results are presented, while extension to 193 nm lithog. is discussed. Very anisotropic and high aspect ratio pattern transfer to Si, with fluorine-only contg. plasmas is demonstrated. Possible applications are discussed.

L84 ANSWER 23 OF 39 HCAPLUS COPYRIGHT 2003 ACS
AN 1996:418065 HCAPLUS
DN 125:102395
TI Degreasing of alumina film in plasma processing of semiconductor **wafers**
IN Machida, Junichi
PA Kokusai Electric Co Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 2 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 08124920	A2	19960517	JP 1994-265466	19941028
PRAI	JP 1994-265466		19941028		

AB A process for degreasing a alumina film in plasma processing of semiconductor **IC wafers**, wherein the solvent consists of org. solvents and H2O, in lieu of the conventional caustic soda, whereby the deposition of contaminants on the **wafer** surface is suppressed.

L84 ANSWER 24 OF 39 HCAPLUS COPYRIGHT 2003 ACS
AN 1996:335240 HCAPLUS
DN 125:46187
TI Defect characterization on a batch clean process used after plasma metal **etching**
AU Mautz, K. E.
CS Motorola Inc., Semiconductor Products Sector, Austin, TX, 78704, USA
SO Proceedings - Electrochemical Society (1996), 95-20(Cleaning Technology in Semiconductor Device Manufacturing), 401-408
CODEN: PESODO; ISSN: 0161-6374
PB Electrochemical Society
DT Journal
LA English
AB Defectivity addn. on batch spray tool clean processes used after plasma metal **etching** was characterized. The defects studied were particulate and veil polymers on the **wafer** surface. Designed expts. were run on the process and equipment factors of the batch spray tool. Particle addns. due to the spray tool recipe were reduced by process and equipment improvements. The clean soln. step was characterized for oxide film removal **etch** and nonuniformity. **Wafer** streaking defects were identified and eliminated by changes in the clean process recipe.

L84 ANSWER 25 OF 39 HCAPLUS COPYRIGHT 2003 ACS
AN 1995:1003018 HCAPLUS
DN 124:73857

TI Method for cleaning the **etching** chamber of a dry **etching** systems
IN Kawamoto, Hiedaki
PA NEC Corporation, Japan
SO U.S., 4 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 5468686	A	19951121	US 1994-351074	19941130
JP 1993-301373		19931201		

AB The method, in which a single semiconductor **wafer** is **etched** and .gtoreq.1 auxiliary chambers are connected to the **etching** chamber via a gate valve, comprises (a) introducing halogen gas into the **etching** chamber to plasma **etch** a single semiconductor **wafer** coated with an Al film and a resist film (on the Al film) in a desired pattern, (b) replacing, while leaving the **wafer** in the **etching** chamber, the halogen gas with an O-contg. cleaning gas capable of removing remaining Cl to thereby generate plasma, and (c) effecting dry **etching** in the **etching** chamber without exposure to the atm. The **etching** and cleaning steps are completed within the time required for the ashing step. This method not only protects the resulting Al wiring on the **wafer** from corrosion, but also saves time otherwise consumed by the cleaning step, thereby increasing the throughput of the system.

L84 ANSWER 26 OF 39 HCAPLUS COPYRIGHT 2003 ACS
AN 1995:990721 HCAPLUS
DN 124:19768
TI Plasma treatment method and apparatus.
IN Tomoyasu, Masayuki; Koshiishi, Akira; Imafuku, Kosuke; Endo, Shosuke; Tahara, Kazuhiro; Naito, Yukio; Nagaseki, Kazuya; Hirose, Keizo; Komino, Mitsuaki; et al.
PA Tokyo Electron Ltd., Japan; Tokyo Electron Yamanashi Ltd.
SO Eur. Pat. Appl., 42 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 2

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
EP 678903	A1	19951025	EP 1995-105916	19950420
R: DE, FR, GB, IT, NL				
JP 07263361	A2	19951013	JP 1994-79541	19940325
JP 3004165	B2	20000131		
JP 07297175	A2	19951110	JP 1994-106045	19940420
JP 3162245	B2	20010425		
JP 07302786	A2	19951114	JP 1994-113587	19940428
JP 3062393	B2	20000710		
JP 2000188286	A2	20000704	JP 2000-13920	19940428
JP 3328625	B2	20020930		
JP 07321097	A2	19951208	JP 1994-133638	19940524
JP 3208008	B2	20010910		
JP 07331445	A2	19951219	JP 1994-142409	19940601
US 5900103	A	19990504	US 1995-424127	19950419
EP 930642	A1	19990721	EP 1999-105170	19950420
EP 930642	B1	20020731		
R: DE, FR, GB, IT, NL				
EP 1207546	A2	20020522	EP 2001-126593	19950420

	R: DE, FR, GB, IT, NL				
	US 6106737	A	20000822	US 1998-94451	19980610
	US 6264788	B1	20010724	US 2000-556133	20000421
	US 2001013504	A1	20010816	US 2000-738302	20001215
	US 6391147	B2	20020521		
	US 2001023744	A1	20010927	US 2001-864022	20010523
	US 6379756	B2	20020430		
	US 6431115	B1	20020813	US 2001-863860	20010523
	US 2001027843	A1	20011011		
	US 2002088547	A1	20020711	US 2002-79600	20020219
	US 6544380	B2	20030408		
PRAI	JP 1994-79541	A	19940325		
	JP 1994-106045	A	19940420		
	JP 1994-113587	A	19940428		
	JP 1994-133638	A	19940524		
	JP 1994-142409	A	19940601		
	US 1995-424127	A3	19950419		
	EP 1995-105916	A3	19950420		
	EP 1999-105170	A3	19950420		
	US 1998-94451	A3	19980610		
	US 2000-556133	A3	20000421		
	US 2001-864022	A1	20010523		

AB A plasma treatment method comprises exhausting a process chamber, mounting a substrate (esp. a semiconductor **wafer**) on a susceptor, supplying a process gas to the **wafer** through a shower electrode, applying high-frequency power, of a 1st frequency lower than the inherent lower ion transit frequencies of the process gas, to the susceptor, and applying high-frequency power, of a 2nd frequency higher than the inherent upper ion transit frequencies of the process gas, whereby a plasma is generated in the chamber and activated species influence the **wafer**.

L84 ANSWER 27 OF 39 HCAPLUS COPYRIGHT 2003 ACS
AN 1995:839805 HCAPLUS
DN 123:327497
TI Micromachined AFM transducer with differential capacitive read-out
AU Bay, Jesper; Bouwstra, Siebe; Lssgsgaard, Erik; Hansen, Ole
CS Microelectronics Centre (MIC), Technical University Denmark (DTU), Lyngby, DK-2800, Den.
SO Journal of Micromechanics and Microengineering (1995), 5(2), 161-5
CODEN: JMMIEZ; ISSN: 0960-1317
PB Institute of Physics
DT Journal
LA English
AB A differential capacitive at. force microscope (AFM) transducer with integrated tip for use in ultra-high vacuum is presented. It is fabricated by the dissolved **wafer** technique with multiple **etch** stop using highly B-doped epitaxial layers. The tip is fabricated using anisotropic **etching** and radii of curvature of the order of 60 nm were measured. Measured sensitivities agree well with the presented model.

L84 ANSWER 28 OF 39 HCAPLUS COPYRIGHT 2003 ACS
AN 1995:754197 HCAPLUS
DN 123:328800
TI Monolithic thin-film metal-oxide gas-sensor arrays with application to monitoring of organic vapors
AU Wang, Xiaodong; Carey, W. Patrick; Yee, Sinclair S.
CS Department of Electrical Engineering FT-10, University of Washington, Seattle, WA, 98195, USA
SO Sensors and Actuators, B: Chemical (1995), B28(1), 63-70

CODEN: SABCEB; ISSN: 0925-4005
PB Elsevier
DT Journal
LA English
AB This paper presents the study of eight-element gas-microsensor arrays that have been developed by silicon-based microfabrication and micromachining techniques combined with the reactive **sputtering** and **etching** of tin(IV) oxide or tin dioxide, zinc oxide, and tungsten trioxide. The mixed metal-oxide array has been fabricated on a 3 mm.times.3 mm silicon **chip**. The process-compatibility problem encountered when delineating multiple sensing materials into a single device is resolved by combining ion-beam milling, 'lift-off', and wet chem. **etching** methods. The microsensor arrays are used to monitor benzene, toluene, and **methanol** and to analyze benzene-toluene mixts. with various multivariate calibration methods. The range of sensitivity of the arrays is tested with concns. between 50 and 500 ppm of the org. vapors. Prediction errors for benzene-toluene mixts. are 29.8 ppm and 17.0 ppm, resp., using projection pursuit regression.

L84 ANSWER 29 OF 39 HCAPLUS COPYRIGHT 2003 ACS
AN 1995:727187 HCAPLUS
DN 123:240186
TI Electrochemical aspects of corrosion resistance and **etching** of metalizations for **microelectronics**
AU Comizzoli, R. B.; Frankenthal, R. P.; Hanson, K. J.; Konstadinidis, K.; Opila, R. L.; Sapjeta, J.; Sinclair, J. D.; Takahashi, K. M.; Frank, A. L.; et al.
CS AT and T Bell Laboratories, Murray Hill, NJ, 07974, USA
SO Materials Science & Engineering, A: Structural Materials: Properties, Microstructure and Processing (1995), A198(1-2), 153-60
CODEN: MSAPE3; ISSN: 0921-5093
PB Elsevier
DT Journal
LA English
AB The electrochem. aspects of metal **etching** to form patterned conductors and of corrosion of conductors in the field are closely related. Both need to be considered in designing metalization structures for **microelectronic** devices. The evolution of a manufg. process for a multilevel interconnect structure is discussed from an electrochem. perspective. A galvanic corrosion problem during manuf. and its soln. for the interconnect metalization on a Si **integrated circuit** are also discussed. Following the discussion on **etching** processes and corrosion during manuf., a discussion of electrochem. and electrolytic failure mechanisms for electronic equipment in field environments and some steps that can be taken to prevent harmful environmental effects are presented. Recent research on the adhesion of various protective coatings and interlevel polymeric dielecs. is presented in the context of failure prevention.

L84 ANSWER 30 OF 39 HCAPLUS COPYRIGHT 2003 ACS
AN 1995:176926 HCAPLUS
DN 122:21345
TI Fabrication of self-aligned GaAs/AlGaAs and GaAs/InGaP microwave power heterojunction bipolar transistors
AU Ren, F.; Lothian, J. R.; Pearton, S. J.; Abernathy, C. R.; Wisk, P. W.; Fullowan, T. R.; Tseng, B.; Chu, S. N. G.; Chen, Y. K.; et al.
CS AT and T Bell Lab., Murray Hill, NJ, 07974, USA
SO Journal of Vacuum Science & Technology, B: Microelectronics and Nanometer Structures (1994), 12(5), 2916-28
CODEN: JVTBD9; ISSN: 0734-211X
PB American Institute of Physics

DT Journal
LA English
AB Self-aligned processing of high efficiency power heterojunction bipolar transistors (HBTs) using implant isolation, selective wet and dry **etching** for mesa formation, plasma-enhanced chem. vapor deposited SiNx for sidewall spacers and through-**wafer** via connections is reported. GaAs/AlGaAs and GaAs/InGaP HBTs grown by metalorg. MBE using C for high, well-confined base doping produced power-added efficiencies of 63%, power gain of 10 dB and output power of 1.7 W at 4 GHz for twelve 2 .times. 15 .mu.m2 double-emitter finger devices (GaAs/AlGaAs) and 57% power-added efficiency, power gain of 11.3 dB and output power of 0.6 W at 4 GHz (GaAs/InGaP), resp.

L84 ANSWER 31 OF 39 HCAPLUS COPYRIGHT 2003 ACS
AN 1994:643450 HCAPLUS
DN 121:243450
TI Dry **etching** of copper thin film
IN Kondo, Hidekazu; Tokunaga, Kyoji
PA Kawasaki Steel Co, Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 06204186	A2	19940722	JP 1992-348656	19921228
	JP 3256707	B2	20020212		
PRAI	JP 1992-348656		19921228		

AB The method is reactive ion **etching** of a Cu thin film using an **etching** gas contg. mixt. of Group VA element hydride and C compd. selected from alc., ether, and ketone. The method enables high-speed **etching** of Cu, and is applied in fabrication of semiconductor **integrated circuits**. Thus, a gas mixt. of PH3 and MeOH was used in the **etching**.

L84 ANSWER 32 OF 39 HCAPLUS COPYRIGHT 2003 ACS
AN 1994:523182 HCAPLUS
DN 121:123182
TI Selective removal of organometallic and organosilicon residues and damaged oxides from semiconductor **wafers**
IN Bowden, Bill; Switalski, Debbie
PA Advanced Chemical Systems International Inc., USA
SO U.S., 5 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5320709	A	19940614	US 1993-21799	19930224
	JP 06295898	A2	19941021	JP 1994-50027	19940224
	JP 2979284	B2	19991115		
PRAI	US 1993-21799		19930224		

AB Oxidized organometallic residues, oxidized organosilicon residues, native oxides, and damaged oxides created in plasma **etching** are selectively removed by immersion of plasma-**etched** Si **wafers** in a soln. of anhyd. NH4F and a polyhydric alc., which is substantially free of HF and H2O.

L84 ANSWER 33 OF 39 HCAPLUS COPYRIGHT 2003 ACS

AN 1994:522570 HCAPLUS
DN 121:122570
TI Cleaning of silicon surface after RIE using UV/ozone and HF/CH3OH
AU Hwang, David K.; Ruzyllo, Jerzy; Kamieniecki, Emil
CS Electron. Mater. Process. and Res. Lab., Pa. State Univ., University Park, PA, 16802, USA
SO Proceedings - Electrochemical Society (1994), 94-7(PROCEEDINGS OF THE THIRD INTERNATIONAL SYMPOSIUM ON CLEANING TECHNOLOGY IN SEMICONDUCTOR DEVICE MANUFACTURING, 1993), 401-8
CODEN: PESODO; ISSN: 0161-6374
DT Journal
LA English
AB The removal of a polymer-like film deposited by a fluorocarbon -based reactive ion **etching** (RIE) chem. using UV/Ozone followed in-situ by an HF/CH3OH oxide **etch** was investigated. The two step cleaning is accomplished in a prototype of a cluster-tool compatible dry cleaning module. RIE on bare silicon **wafers** using a CHF3 chem. was performed to simulate an overetch process. The change in the polymer thickness during the UV/Ozone removal process was monitored using an ellipsometer. XPS results indicate a significant redn. in the carbon, fluorine and oxygen content on the silicon surface after the cleaning process. Surface charge anal. (SCA) was also used to compare the surface condition of the **etched** and cleaned sample with an unetched sample.

L84 ANSWER 34 OF 39 HCAPLUS COPYRIGHT 2003 ACS
AN 1994:497821 HCAPLUS
DN 121:97821
TI Dry **etching** method
IN Kanekiyo, Tadamitsu; Kawahara, Hironobu; Sato, Yoshiaki; Fujimoto, Kotaro
PA Hitachi, Ltd., Japan
SO U.S., 36 pp. Cont.-in-part of U.S. Ser. No. 978,171.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 4

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5320707	A	19940614	US 1993-63983	19930520
	JP 02224233	A2	19900906	JP 1989-42976	19890227
	JP 2528962	B2	19960828		
	US 5007981	A	19910416	US 1990-477474	19900209
	US 5200017	A	19930406	US 1991-638378	19910107
	JP 05217966	A2	19930827	JP 1992-17997	19920204
	US 5868854	A	19990209	US 1992-987171	19921208
	JP 09237821	A2	19970909	JP 1997-51455	19970306
	JP 3098203	B2	20001016		
	US 2002013063	A1	20020131	US 2001-917912	20010731
	US 2002023720	A1	20020228	US 2001-985308	20011102
	US 6537417	B2	20030325		
PRAI	JP 1989-42976	A	19890227		
	US 1990-477474	A3	19900209		
	US 1991-638378	A2	19910107		
	JP 1992-17997	A	19920204		
	JP 1992-281320	A	19921020		
	US 1992-987171	A2	19921208		
	JP 1996-12724	A3	19890227		
	US 1995-470443	B1	19950606		
	US 2001-847406	A3	20010503		

OS MARPAT 121:97821
AB Described is a method of dry-**etching** a sample (e.g., a

wafer) having an Al system film structure. **Etching** is performed under reduced pressure in a plasma formed from a gas mixt. contg. a halogen system gas (e.g., Cl2, HBr, BCl3, etc.) and a ROH gas (e.g., CH3OH, C3H5OH, C5H7OH, CH3COOH, HOCH2CH2OH, etc.). By incorporating the ROH gas with the halogen system gas, in **etching** the Al system film structure, **etching** can be performed within an accurate shape corresponding to a mask pattern, irresp. of the pattern d.

L84 ANSWER 35 OF 39 HCAPLUS COPYRIGHT 2003 ACS
AN 1993:660739 HCAPLUS
DN 119:260739
TI Manufacture of semiconductor device by dry **etching**
IN Hanaoka, Hideyasu
PA Seiko Epson Corp, Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 05109673	A2	19930430	JP 1991-272758	19911021
PRAI	JP 1991-272758		19911021		

AB The device is manufd. by dry **etching** an Al (alloy) monolayer or multilayer wiring on a **wafer** and resist ashing at .ltoreq.100.degree.. Curing of a sidewall protecting film was prevented.

L84 ANSWER 36 OF 39 HCAPLUS COPYRIGHT 2003 ACS
AN 1993:90636 HCAPLUS
DN 118:90636
TI Wet silylation and dry development with the AZ 5214 photoresist
AU Gogolides, Evangelos; Tsoi, Elizabeth; Nassiopoulos, Androula G.; Hatzakis, Michael
CS Inst. Microelectron., NCSR "Demokritos", Agia Paraskevi, 153 10, Greece
SO Journal of Vacuum Science & Technology, B: Microelectronics and Nanometer Structures (1992), 10(6), 2610-14
CODEN: JVTBD9; ISSN: 0734-211X
DT Journal
LA English
AB A pos. tone surface imaging process using wet silylation and dry development of AZ 5214 photoresist was developed. The process steps are spinning and prebake of the photoresist, i-line exposure, postexposure bake, wet silylation, and dry development in O2 plasma. The process was developed using statistically designed expts., starting with a Placket-Burman screening exptl. design for 6 variables. The compn. of the silylating soln. was the most important variable. As a result, a mixt. exptl. design followed, with the concns. of the silylating agent and solvents as the only variables. Characterization of the process and process window definition were done with UV spectroscopy of films made on quartz **wafers**, and SEM photographs.

L84 ANSWER 37 OF 39 HCAPLUS COPYRIGHT 2003 ACS
AN 1989:565482 HCAPLUS
DN 111:165482
TI Reactive ion **etching** of layer containing indium oxide
IN Kawaguchi, Takao; Minamino, Yutaka; Okawa, Noriko; Takeda, Yoshiya; Nagata, Seiichi
PA Matsushita Electric Industrial Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent

LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 64000285	A2	19890105	JP 1987-155871	19870623
PRAI	JP 1987-155871		19870623		

AB The title method involves using an **etching** gas contg. .gtoreq.1 gas of an alc. and carboxylic acid and .gtoreq.1 of N, Ar, and He 0-20%, and maintaining a gas pressure at the silent-discharge period to <5 Pa. The method utilizes a simple gas such as an alc. or carboxylic acid. The method is useful for manufg. an **integrated circuit**.

L84 ANSWER 38 OF 39 HCAPLUS COPYRIGHT 2003 ACS
AN 1988:443904 HCAPLUS
DN 109:43904
TI Quantitative reflection high-energy electron diffraction measurements of surface roughness in gallium arsenide(100)
AU Heller, E. J.; Savage, D. E.; Lagally, M. G.
CS Dep. Metall. Miner. Eng., Univ. Wisconsin, Madison, WI, 53706, USA
SO Journal of Vacuum Science & Technology, A: Vacuum, Surfaces, and Films (1988), 6(3, Pt. 2), 1484-5
CODEN: JVTAD6; ISSN: 0734-2101
DT Journal
LA English
AB RHEED (RHEED) measurements of the microscopic surface roughness of polished GaAs(100) **wafers** subjected to various surface cleaning procedures are presented. These include Br2:MeOH, HCl, and **sputter etching**, each followed by annealing in ultrahigh vacuum. The results indicate that chem. **etches** such as Br2:MeOH and HCl produce large 3-dimensional asperities that cannot be removed by annealing, while **sputter etching** produces less roughness. Quant. values of the mean asperity height are presented. Measurements on GaAs(100) are compared with results from **sputter -etching**-induced roughness on cleaved GaAs(100), which initially has a nearly defect-free surface. Remanent roughness is always .gtoreq.2 or 3 at. layers, with terrace widths of .ltoreq.100 .ANG..

L84 ANSWER 39 OF 39 HCAPLUS COPYRIGHT 2003 ACS
AN 1982:95814 HCAPLUS
DN 96:95814
TI Multilevel resist for lithography below 100 nm
AU Howard, Richard E.; Hu, Evelyn L.; Jackel, Lawrence D.
CS Bell Lab., Holmdel, NJ, 07733, USA
SO IEEE Transactions on Electron Devices (1981), ED-28(11), 1378-81
CODEN: IETDAI; ISSN: 0018-9383
DT Journal
LA English
AB Two- and 3-level resist systems are described for electron-beam lithog. of Si for circuit patterns with features as fine as 25 nm. The 2-layer resist consists of a copolymer of Me methacrylate and methacrylic acid and an upper layer of poly(Me methacrylate). The resist is developed by an ethylene **glycol** monoethyl ether soln. in MeOH. The 3-level resist has a layer of Ge between the 2 layers. The top polymer is developed as above, the Ge is patterned by a CF4 plasma, and the lower layer is **etched** by an O plasma. Au and Ni-Cr lines of .apprx.25 nm were formed.

L88 ANSWER 1 OF 9 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:586630 HCAPLUS
DN 137:331482
TI A copper interconnect process for the 130-nm process technology node
AU Moon, P.; Allen, C.; Anand, N.; Austin, D.; Bramblett, T.; Fradkin, M.; Fu, S.; Hussein, M.; Jeong, J.; Lo, C.; Ott, A.; **Smith, P.**; Rumaner, L.
CS Portland Technology Development, Intel Corporation, Hillsboro, OR, 97124-6497, USA
SO Advanced Metallization Conference 2001, Proceedings of the Conference, Montreal, Canada, Oct. 8-11 and a Parallel Session of the Conference, Tokyo, Japan, Oct. 29-31, 2001 (2002), Meeting Date 2001, 39-41. Editor(s): McKerrow, Andrew J. Publisher: Materials Research Society, Warrendale, Pa.
CODEN: 69CXX3; ISBN: 1-55899-670-2
DT Conference
LA English
AB This paper describes Intel's interconnect process for the 130-nm logic process technol. generation which uses dual damascene copper interconnects and fluorosilicate glass (FSG) interlevel dielec. Metal pitches are 350-nm at the top layer. This process is currently ramping into high vol. prodn. on 200-mm **wafers** and demonstrating high yield on both 200-mm and 300-mm **wafers**.
RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L88 ANSWER 2 OF 9 HCAPLUS COPYRIGHT 2003 ACS
AN 2002:358147 HCAPLUS
DN 136:348762
TI Formation of AlN films on Ti/TiN ARC-layer interface with Al-0.5% Cu interconnects evaluated by XPS and energy-filtered TEM
AU Gazda, J.; Zhao, J.; **Smith, P.**; White, R. A.
CS Process Characterization Laboratory, Advanced Micro Devices Corporation, Austin, TX, 78741, USA
SO Materials Research Society Symposium Proceedings (2001), 589(Advances in Materials Problem Solving with the Electron Microscope), 365-370
CODEN: MRSPDH; ISSN: 0272-9172
PB Materials Research Society
DT Journal
LA English
AB Titanium/titanium nitride antireflective coatings (ARC) are widely used in the semiconductor industry during photolithog. of aluminum metal interconnect lines. The quality and effectiveness of these coatings, however, depend strongly on the ability to control reaction products formed at film interfaces during processing. In the present study, formation of an Al-N compd. at the interface between Ti/TiN ARC/BARC and Al-(0.5 wt.%)Cu interconnect was investigated. The effects of deposition temps. for individual films and ensuing thermal cycling of the whole metal stack on the formation of intermetallics were evaluated. The compn. and chem. bonding state of an aluminum nitride interfacial layer was evaluated by XPS of blanket **wafers**. These results are combined with measurements made by energy-filtered TEM microscopy (EFTEM) of thickness and continuity of the film in specimens prepd. by focused ion beam milling (FIB). The formation of AlN depends on the thermal cycling history of the metal stacks.
RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L88 ANSWER 3 OF 9 HCAPLUS COPYRIGHT 2003 ACS
AN 1992:643273 HCAPLUS

DN 117:243273
TI Resistance and structural stabilities of epitaxial cobalt disilicide films on (001) silicon substrates
AU Hsia, S. L.; Tan, T. Y.; **Smith, P.**; McGuire, G. E.
CS Dep. Mech. Eng. Mater. Sci., Duke Univ., Durham, NC, 27706, USA
SO Journal of Applied Physics (1992), 72(5), 1864-73
CODEN: JAPIAU; ISSN: 0021-8979
DT Journal
LA English
AB The resistance and structural stabilities of the epitaxial CoSi2 films, grown on (001) Si substrates using sequentially deposited Ti-Co bimetallic layer source materials, have been investigated by further anneals under extended conditions. In contrast to reported polycryst. silicide film cases, the epitaxial CoSi2 films are very stable under the addnl. rapid thermal annealing treatment at 1100.degree.C for times from 10 to 60 s. This means that such CoSi2 films are able to stand the further heat treatment required in the ultralarge-scale integration regime of Si **integrated circuit** fabrication. The quality of the further annealed films has been actually improved:. The film resistivity has decreased to reach a value as low as 10 .mu..OMEGA. cm, and the film structure has become more perfect, e.g., the densities of antiphase domains and film-Si interface facets has been decreased. For technol. applications, it is necessary to remove the Ti-Co-Si alloy layer formed concomitantly on top of the as-grown CoSi2 film. This has been accomplished by chem. etching using the std. buffered oxide etch soln. In the present expt., as-grown epitaxial CoSi2 films with and without the Ti-Co-Si alloy top layers have been both included and the same film resistance and structural stabilities have been obsd. Thus, the excellent resistance and structural thermal stabilities of the present CoSi2 films result from the single-crystal nature of the films and not the effect of the top Ti-Co-Si capping layer. Mechanisms responsible for the excellent quality of the epitaxial CoSi2 films, as well as for the unacceptable quality of the polycryst. silicide films, have been discussed.

L88 ANSWER 4 OF 9 HCAPLUS COPYRIGHT 2003 ACS
AN 1992:96674 HCAPLUS
DN 116:96674
TI Formation of epitaxial cobalt disilicide films on (001) silicon using titanium-cobalt alloy and bimetal source materials
AU Hsia, S. L.; Tan, T. Y.; **Smith, P.**; McGuire, G. E.
CS Dep. Mech. Eng. Mater. Sci., Duke Univ., Durham, NC, 27706, USA
SO Journal of Applied Physics (1991), 70(12), 7579-87
CODEN: JAPIAU; ISSN: 0021-8979
DT Journal
LA English
AB Using coevapd. Ti-Co alloy and sequentially Ti-Co bimetallic layer source materials, CoSi2 films have been grown on (001) Si. The film resistivity and resistance thermal stability are excellent. The epitaxial nature of the CoSi2 films results from two roles played by Ti. In the first, Ti served as a getterer for removing the native oxide layer on the Si **wafer** surfaces, which causes the nucleation of CoSi2 grains with random orientations. In the second, Ti silicides, formed in the early stage of the annealing process, served as Co diffusion barriers preventing Co2Si and CoSi formation, which would also lead to the formation of randomly oriented CoSi2 grains. Models of the interfacial structure of the epitaxial CoSi2 film and Si substrate have been constructed for [001] and [111] orientations. These models revealed that antiphase boundaries serve the role of relieving the lattice mismatch between the epitaxial CoSi2 film and si substrate.

L88 ANSWER 5 OF 9 HCAPLUS COPYRIGHT 2003 ACS

AN 1990:415673 HCAPLUS
DN 113:15673
TI Gettering phenomena in directly bonded silicon **wafers**
AU Yang, W. S.; Ahn, K. Y.; Li, J.; **Smith, P.**; Tan, T. Y.; Gosele, U.
CS Sch. Eng., Duke Univ., Durham, NC, 27706, USA
SO Proceedings - Electrochemical Society (1990), 90-7(Semicond. Silicon 1990), 628-38
CODEN: PESODO; ISSN: 0161-6374
DT Journal
LA English
AB Gold and copper gettering was investigated near the bonding interface of directly bonded silicon **wafers**. Boron-doped (100) float-zone silicon **wafers** were rotationally misoriented against each other by 1.degree., 25.degree. or 6.degree., and then bonded and annealed at 1100.degree. for 2 h. Then a thin film of gold or copper was deposited on only one side of the bonded **wafers**, and annealed for 3 h at 950.degree. and 1000.degree. for gold diffusion, and 900.degree. and 1100.degree. for copper diffusion. Spreading resistance measurements and TEM were used, resp., to check for gettering phenomena of gold and copper. The results showed that the gold concn. had increased, and that copper had pptd. near the bonding interface. These results indicate that the bonding interface of bonded **wafers** can provide gettering sites for metallic impurities and can therefore be used for introducing a gettering layer at a controlled distance from the active device region.

L88 ANSWER 6 OF 9 HCAPLUS COPYRIGHT 2003 ACS
AN 1990:205478 HCAPLUS
DN 112:205478
TI TEM investigation of interfacial oxide layers between directly bonded silicon **wafers**
AU Ahn, K. Y.; Stengl, R.; Gosele, U.; **Smith, P.**
CS Sch. Eng., Duke Univ., Durham, NC, 27706, USA
SO Institute of Physics Conference Series (1989), 100(Microsc. Semicond. Mater.), 569-74
CODEN: IPCSEP; ISSN: 0951-3248
DT Journal
LA English
AB The influence of the O interstitial concn. and that of the crystallog. misorientation on the interfacial oxide layer between directly bonded Si **wafers** were investigated by transmission electron microscopy. **Wafers** with different concns. of oxygen interstitials were bonded or rotated around their common axis perpendicular to the **wafer** plane and bonded. Depending on the starting concns. of O interstitials in the **wafer**, the interfacial oxide layer grows or shrinks. If the rotational angle is larger than a crit. value, the disintegration of the interfacial oxide layers is energetically less favorable than keeping a continuous oxide layer. The crit. angle to keep a continuous oxide layer is detd. to be between 1 and 3.degree..

L88 ANSWER 7 OF 9 HCAPLUS COPYRIGHT 2003 ACS
AN 1990:169994 HCAPLUS
DN 112:169994
TI Growth, shrinkage, and stability of interfacial oxide layers between directly bonded silicon **wafers**
AU Ahn, K. Y.; Stengl, R.; Tan, T. Y.; Gosele, U.; **Smith, P.**
CS Sch. Eng., Duke Univ., Durham, NC, 27706, USA
SO Applied Physics A: Solids and Surfaces (1990), A50(1), 85-94
CODEN: APSFDB; ISSN: 0721-7250
DT Journal
LA English

AB Models for the growth and shrinkage of an interfacial oxide layer and for the stability of the interfacial oxide layer are formulated. Predictions of these models are compared to results obtained by high-resoln. transmission electron microscopy. **Wafers** contg. different concns. of O interstitials are bonded. Depending on the starting concn. of O interstitials in the **wafers**, the interfacial oxide layer grows or shrinks during long-time annealing at high temps. For much shorter annealing times, local disintegration of the oxide layer may occur, which is less severely influenced by the concn. of oxygen interstitials. Rather, it depends on the thickness of the interfacial oxide layer. The influence of rotational misorientation is examd. by rotating **wafers** around their common axes perpendicular to a **wafer** plane and subsequent bonding. Above a crit. angle of about 1-3.degree., a continuous oxide layer is formed, whereas below this crit. angle, sufficiently thin oxide layers disintegrate.

L88 ANSWER 8 OF 9 HCAPLUS COPYRIGHT 2003 ACS
AN 1989:106066 HCAPLUS
DN 110:106066
TI Stability of interfacial oxide layers during silicon **wafer** bonding
AU Ahn, K. Y.; Stengl, R.; Tan, T. Y.; Goesele, U.; **Smith, P.**
CS Sch. Eng., Duke Univ., Durham, NC, 27706, USA
SO Journal of Applied Physics (1989), 65(2), 561-3
CODEN: JAPIAU; ISSN: 0021-8979
DT Journal
LA English
AB The stability of thin interfacial oxide layers between bonded Si **wafers** was investigated exptl. and theor. For usual bonding temps. around 1100.degree. and typical times of a few hours, the O diffusivity is not high enough to allow oxide layer dissoln. For aligned **wafers** of the same orientation, the oxide layer instead tends to disintegrate in order to minimize the SiO2/Si interface energy. It is possible to stabilize a uniform interfacial oxide layer by rotationally misorienting the 2 **wafers** by an angle .theta. exceeding a crit. angle, .theta.crit., estd. to be between 1.degree. and 5.degree..

L88 ANSWER 9 OF 9 HCAPLUS COPYRIGHT 2003 ACS
AN 1983:117792 HCAPLUS
DN 98:117792
TI High-speed gallium aluminum arsenide-gallium arsenide heterojunction bipolar transistors with near-ballistic operation
AU Ankri, D.; Schaff, W. J.; **Smith, P.**; Eastman, L. F.
CS Sch. Electric. Eng., Cornell Univ., Ithaca, NY, 14853, USA
SO Electronics Letters (1983), 19(4), 147-9
CODEN: ELLEAK; ISSN: 0013-5194
DT Journal
LA English
AB (Ga,Al)As-GaAs heterojunction bipolar transistors with an abrupt emitter-base interface were realized by mol.-beam epitaxy on semi-insulating substrates. A gain-bandwidth product FT of 15 GHz was measured for **Ic** = 20 mA and VCE = 8 V. These results are the best reported so far for heterostructure bipolar transistors and are very promising for high-speed logic.

L115 ANSWER 1 OF 25 WPIX (C) 2003 THOMSON DERWENT
AN 2003-156414 [15] WPIX
DNN N2003-123499 DNC C2003-040509
TI Silicon dioxide low-k dielectric stack formation for multilevel interconnect formation, involves forming cap layer on dielectric layer after applying **hydrogen plasma**.
DC A85 L03 U11 U13
IN CHANG, T; LIU, P; MOR, Y
PA (CHAN-I) CHANG T; (LIUP-I) LIU P; (MORY-I) MOR Y
CYC 1
PI US 2002164868 A1 20021107 (200315)* 7p
ADT US 2002164868 A1 US 2001-847087 20010502
PRAI US 2001-847087 20010502
AB US2002164868 A UPAB: 20030303
NOVELTY - A low k dielectric layer (22) is formed over a conductive interconnect layer (20) having Al lines. An H2 plasma (23) is applied on the low k dielectric layer and then a cap layer of silicon dioxide is formed on the low k dielectric layer.
USE - For forming silicon dioxide-low k dielectric stack for multilevel interconnection in ultra large scale **integrated circuits** (ULSI).
ADVANTAGE - The H2 plasma treatment can effectively prevent oxygen gas from damaging the low k dielectric layer, during the process for forming the cap layer of silicon dioxide, thus silicon dioxide-low k dielectric stack can be formed with high reliability.
DESCRIPTION OF DRAWING(S) - The figure shows a schematic cross-sectional view of the dielectric stacked structure formation process.
Conductive interconnect layer 20
Low k dielectric layer 22
H2 plasma 23
Dwg.2B/3

L115 ANSWER 2 OF 25 WPIX (C) 2003 THOMSON DERWENT
AN 2003-017772 [01] WPIX
CR 2002-215896 [27]; 2002-607112 [65]
DNN N2003-013655 DNC C2003-004242
TI Semiconductor **wafer** cleaning formulation for semiconductor fabrication, comprises organic amine(s), water, chelating agent(s), nitrogen-containing carboxylic acid or imine and polar organic solvent.
DC L03 U11
IN BERNHARD, D; NGUYEN, L; SEIJO, M F; WOJTCZAK, W A
PA (BERN-I) BERNHARD D; (NGUY-I) NGUYEN L; (SEIJ-I) SEIJO M F; (WOJT-I) WOJTCZAK W A
CYC 1
PI US 2002132744 A1 20020919 (200301)* 10p
ADT US 2002132744 A1 CIP of US 2000-732370 20001208, US 2001-7490 20011205
FDT US 2002132744 A1 CIP of US 6344432
PRAI US 2001-7490 20011205; US 2000-732370 20001208
AB US2002132744 A UPAB: 20030101
NOVELTY - A semiconductor **wafer** cleaning formulation comprises organic amine(s) (in weight%) (2-98), water (0-50), 1,3-dicarbonyl compound chelating agent (0.1-60), additional different chelating agent(s) (0-25), nitrogen-containing carboxylic acid or imine (0.1-40) and polar organic solvent (2-98).
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:
(1) Method for fabricating semiconductor **wafer** which involves plasma etching a metallized layer from a surface of the **wafer**, plasma ashing a resist from the surface of the

wafer and cleaning the **wafer** with the semiconductor **wafer** cleaning formulation; and

(2) Method of removing residue from a **wafer** following a resist plasma ashing step which involves contacting the **wafer** with the cleaning formulation.

USE - For post plasma ashing semiconductor fabrication and for removal of inorganic residue (both claimed) from semiconductor **wafers** containing delicate copper interconnecting structures and for cleaning **wafers** that have been etched with chlorine or fluorine containing plasmas followed by **oxygen plasma** ashing.

ADVANTAGE - The semiconductor **wafer** cleaning formulation effectively removes residue following the resist ashing step. The **wafer** for cleaning formulation does not attack and potentially degrade delicate metal structures that are meant to remain on the **wafer**. The cleaning formulation provides improved corrosion resistance for protection of copper structures on semiconductor substrate. The cleaning formulation is easily rinsed off by water or other rinse media after the completion of residue removal process hence, the contamination of integrated circuitry on the **wafer** substrate is reduced. Therefore, the quality of resulting **microelectronic** device products is improved.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic representation of copper specific corrosion inhibitor which forms a protective layer on the copper metal to prevent corrosion.

Dwg.1/2

L115 ANSWER 3 OF 25 WPIX (C) 2003 THOMSON DERWENT
AN 2002-535434 [57] WPIX
DNN N2002-423834 DNC C2002-151878
TI Intermetal dielectric layer fabrication in high speed **integrated circuit**, involves vaporizing filler material by diffusing it through dielectric layer to form gap between conductive lines.
DC A85 L03 U11 V05
IN ANG, T; LIM, V S K; SEE, A; SIEW, Y K; TEH, Y; LIM, S K V
PA (CHAR-N) CHARTERED SEMICONDUCTOR MFG INC
CYC 30
PI US 6380106 B1 20020430 (200257)* 11p
EP 1209739 A2 20020529 (200257) EN
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR
JP 2002217293 A 20020802 (200266) 8p
KR 2002041304 A 20020601 (200277)
TW 494532 A 20020711 (200328)
ADT US 6380106 B1 US 2000-721719 20001127; EP 1209739 A2 EP 2001-480117 20011123; JP 2002217293 A JP 2001-348198 20011114; KR 2002041304 A KR 2001-73800 20011126; TW 494532 A TW 2001-108866 20010413
PRAI US 2000-721719 20001127
AB US 6380106 B UPAB: 20020906
NOVELTY - A filler material layer (30) is formed on spaced conductive lines (20) on a semiconductor substrate (10) by spin-on process or chemo-mechanical polishing process. A permeable dielectric layer (40) is formed on the filler material at a temperature between 325-375 deg. C. The formation of dielectric layer vaporizes the filler material so that it diffuses through the dielectric layer to form a gap between the conductive lines. An insulating layer is deposited over the dielectric layer.

DETAILED DESCRIPTION - The insulating layer formed on the dielectric layer is planarized by a chemo-mechanical polishing. The filler material formed on conductive lines is made of a material selected from a group consisting of polypropylene **glycol** (PPG), polybutadiene (PB), polyethylene **glycol** (PEG) and polycaprolactone diol (PCL). Etch

back of the filler material is performed by a reactive ion etch (RIE) using an **oxygen plasma**. The filler material is vaporized by shutting-off a silicon content gas flow and continuing the argon and oxygen gas flows on the material. The plasma power is continuously applied on the material to raise the substrate temperature. A helium gas flow to the substrate is stopped. The filler material is also formed by chemical vapor deposition process on fluorinated amorphous carbon.

USE - Used for micro-electronic fabrications of high speed **integrated circuit**, solar cell, ceramic substrate and flat panel display.

ADVANTAGE - Provides easy formation of air gap by diffusion of filler material through permeable membrane. Avoids need for settings of flow rate and pressure for conductive line fabrication.

DESCRIPTION OF DRAWING(S) - The figures show the cross-sectional view illustrating conductive line structure fabrication method.

Semiconductor substrate 10
Conductive lines 20
Filler material layer 30
Permeable dielectric layer 40

Dwg.3, 4/11

L115 ANSWER 4 OF 25 WPIX (C) 2003 THOMSON DERWENT
AN 2002-163037 [21] WPIX
DNN N2002-124409 DNC C2002-050233
TI Patterning and cleaning of freshly etched dual damascene involves ashing **wafer** in plasma containing oxygen and nitrogen, etching in etchant gas plasma containing fluorocarbons, and subjecting to **hydrogen plasma** treatment.
DC L03 U11
IN CHAO, L; CHEN, C; LIU, J; LUI, M; TSAI, C
PA (TASE-N) TAIWAN SEMICONDUCTOR MFG CO
CYC 1
PI US 6323121 B1 20011127 (200221)* 9p
ADT US 6323121 B1 US 2000-570018 20000512
PRAI US 2000-570018 20000512
AB US 6323121 B UPAB: 20020403

NOVELTY - A freshly etched dual damascene is patterned and cleaned via an opening by ashing a **wafer** in a plasma containing oxygen and nitrogen. The etch stop is removed at the base of via opening by plasma etching in an etchant gas plasma containing fluorocarbons. The **wafer** is subjected to **hydrogen plasma** treatment to remove the **polymeric** residue formed by the plasma etching.

DETAILED DESCRIPTION - Patterning and cleaning of freshly etched dual damascene via an opening involves providing a **wafer** (10) having metal pattern (14), etch stop (16, 20) and insulative layer (12), in sequence. The insulative layer is patterned with a photoresist mask, then anistropically etched to the etch stop to form an opening (8). The **wafer** is ashed in a plasma containing oxygen and nitrogen. The etch stop is removed at the base of via opening by plasma etching in an etchant gas plasma containing fluorocarbons. A **polymeric** residue is formed by attack of etchant gas plasma on the metal pattern which is exposed by the etching. The **wafer** is subjected to **hydrogen plasma** treatment to remove the **polymeric** residue. The vacuum is not break during the removal of etch stop and **polymeric** residue.

USE - Patterning and cleaning a freshly etch dual damascene via an opening.

ADVANTAGE - Provides totally anisotropic cleaning action without damaging or contaminating exposed lateral edges of low-k organic and doped

silicaceous structural layers. The method is completely dry so avoiding absorption of moisture or solvents by porous low-k layers (18, 22).

DESCRIPTION OF DRAWING(S) - The drawing shows a cross-section of the silicon **wafer** with formed via.

Opening 8

Wafer 10

Insulating layer 12

Metal pattern 14

Etch stop 16, 20

Low-k layers 18, 22

Dwg.1F/1

L115 ANSWER 5 OF 25 WPIX (C) 2003 THOMSON DERWENT

AN 2000-282850 [24] WPIX

DNN N2000-212899 DNC C2000-085291

TI Periodic porous and relief nanostructured articles have at least first and second periodically occurring domains which are topologically continuous.

DC A14 A89 G06 L03 P84 U11

IN AVGEROPOULOS, A; CHAN, V Z H; HADJICHRISTIDIS, N; LEE, V Y; MILLER, R D; THOMAS, E L

PA (MASI) MASSACHUSETTS INST TECHNOLOGY

CYC 22

PI WO 2000002090 A2 20000113 (200024)* EN 93p

RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE

W: AU CA JP US

AU 9949674 A 20000124 (200027)

ADT WO 2000002090 A2 WO 1999-US15068 19990702; AU 9949674 A AU 1999-49674 19990702

FDT AU 9949674 A Based on WO 200002090

PRAI US 1998-91676P 19980702

AB WO 200002090 A UPAB: 20000522

NOVELTY - The articles have at least first and second periodically occurring domains which are topologically continuous. The first domain comprising a polymer containing an inorganic material capable of forming a ceramic oxide in amount at least 3 atom% based on the total number of atoms in the first domain.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for:

(a) a membrane composed of the above article;

(b) a mould composed of the above article;

(c) a method of producing a periodic structure of the above material, involving filling the void spaces;

(d) a photonic band gap article of the above material;

(e) a low level dielectric constant material of the above structure;

(f) a high level dielectric constant material of the above structure;

(g) a method for forming a magnetic article by adding magnetic material to the void spaces;

(h) the magnetic article produced.

USE - The **polymeric** materials can be used in photoresists for **integrated circuit** production and as oxygen reactive ion etch barriers.

ADVANTAGE - The structures are stable, durable and multifunctional. They are inexpensive and can be mechanically flexible. Different domains can have different compositions and/or set of physical properties.

DESCRIPTION OF DRAWING(S) - The drawing shows a schematic flow diagram of the manufacture of the nanostructured articles.

cylindrical domains 20

polymeric species 22

inorganic ceramic oxide 26

polymeric article 90

substrate surface 97

Dwg.7/19

L115 ANSWER 6 OF 25 WPIX (C) 2003 THOMSON DERWENT
AN 2000-255537 [22] WPIX
DNN N2000-189908 DNC C2000-077902
TI Removal of photoresist from a semiconductor **wafer** comprises an organic solvent rinse, drying, ashing and a post ash rinse without use of an organic solvent during the post ash rinse.
DC G06 L03 P84 U11
IN ATNIP, E V
PA (TEXI) TEXAS INSTR INC
CYC 1
PI US 6030754 A 20000229 (200022)* 8p
ADT US 6030754 A Provisional US 1996-32614P 19961205, US 1997-985593 19971205
PRAI US 1996-32614P 19961205; US 1997-985593 19971205
AB US 6030754 A UPAB: 20000508
NOVELTY - Photoresist is removed from a semiconductor **wafer** by rinsing in an organic solvent, rinsing in light alcohol, vapor drying in light alcohol, ashing, rinsing in light alcohol and vapor drying in light alcohol, the light alcohol being **methanol**, ethanol or isopropanol.
DETAILED DESCRIPTION - The ashing step comprises oxidising in an **oxygen plasma**. The **wafer** includes exposed metal lines and the organic solvent is a solvent selected not to attack the lines. A suitable organic solvent is ACT CMI(RTM).
USE - In fabrication of **integrated circuits** such as DRAM circuits.
ADVANTAGE - The elimination of organic solvent during the post ash rinse reduces solvent demand, processing time and equipment costs, and reduces contamination risk.
DESCRIPTION OF DRAWING(S) - The drawing shows a flow chart of the process of the invention.
Dwg.5/5

L115 ANSWER 7 OF 25 WPIX (C) 2003 THOMSON DERWENT
AN 2000-072457 [06] WPIX
DNN N2000-056692 DNC C2000-020701
TI Formulation for stripping **wafer** residues in semiconductor **wafer** fabrication.
DC E19 L03 P84 U11
IN GUAN, G; NGUYEN, L; WOJTCZAK, W A
PA (ADTE-N) ADVANCED TECHNOLOGY MATERIALS; (GUAN-I) GUAN G; (NGUY-I) NGUYEN L; (WOJT-I) WOJTCZAK W A; (ADCH-N) ADVANCED CHEM SYSTEMS INT INC
CYC 26
PI WO 9960447 A1 19991125 (200006)* EN 15p
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
W: CA ID IL JP KR SG
US 2001008878 A1 20010719 (200143)
EP 1125168 A1 20010822 (200149) EN
R: AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
KR 2001025043 A 20010326 (200161)
US 6306807 B1 20011023 (200165)
JP 2002516476 W 20020604 (200239) 16p
US 6492310 B2 20021210 (200301)
US 2003040447 A1 20030227 (200318)
ADT WO 9960447 A1 WO 1999-US10895 19990517; US 2001008878 A1 Provisional US 1998-85879P 19980518, Cont of US 1999-312933 19990517, US 2001-801543 20010307; EP 1125168 A1 EP 1999-924300 19990517, WO 1999-US10895 19990517; KR 2001025043 A KR 2000-712974 20001118; US 6306807 B1 Provisional US 1998-85879P 19980518, US 1999-312933 19990517; JP 2002516476 W WO 1999-US10895 19990517, JP 2000-550002 19990517; US 6492310 B2 Provisional US 1998-85879P 19980518, Cont of US 1999-312933 19990517, US 2001-801543

20010307; US 2003040447 A1 Provisional US 1998-85879P 19980518, Cont of US 1999-312933 19990517, Div ex US 2001-801543 20010307, US 2002-179867 20020625

FDT EP 1125168 A1 Based on WO 9960447; JP 2002516476 W Based on WO 9960447; US 2003040447 A1 Cont of US 6306807

PRAI US 1998-85879P 19980518; US 1999-312933 19990517; US 2001-801543 20010307; US 2002-179867 20020625

AB WO 9960447 A UPAB: 20000209

NOVELTY - A formulation for stripping **wafer** residues originating from high density plasma metal etching followed by plasma ashing comprises (wt. %):

(1) 2-17% boric acid;

(2) 35-70% organic amine or mixture of amines and 20-45% water or another solvent as primary ingredients; and

(3) 0-5% **glycol** solvent and/or 0-17% chelating agent as optional ingredients.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a method of fabricating the semiconductor **wafer** comprising:

(i) plasma etching of the metallized layer from the surface of the **wafer**;

(ii) plasma ashing a resist from the surface of the **wafer** after metal etching step; and

(iii) cleaning the **wafer** using the chemical formulation.

USE - The formulations is used for stripping **wafer** residues in semiconductor **wafer** fabrication. It is particularly useful on **wafers** which have been etched with chlorine or fluorine-containing plasmas followed by **oxygen plasma** ashing.

ADVANTAGE - The formulation effectively removes inorganic residues like metal halide and metal oxide following the plasma ashing step. It also removes inorganic residues from a semiconductor **wafer** without containing a strong acid or a strong base.

Dwg.0/0

L115 ANSWER 8 OF 25 WPIX (C) 2003 THOMSON DERWENT

AN 1999-430701 [36] WPIX

DNN N1999-320654 DNC C1999-127047

TI Nanoporous silica dielectric films for **integrated circuits**.

DC A85 G02 L03 P42 U11

IN DRAGE, J S; FORESTER, L; YANG, J

PA (ALLC) ALLIED-SIGNAL INC

CYC 83

PI WO 9936953 A1 19990722 (199936)* EN 34p

RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW

W: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW

AU 9923277 A 19990802 (199954)

US 6042994 A 20000328 (200023)

EP 1050075 A1 20001108 (200062) EN

R: DE FR GB IE NL

KR 2001024873 A 20010326 (200161)

TW 466636 A 20011201 (200252)

ADT WO 9936953 A1 WO 1999-US1119 19990119; AU 9923277 A AU 1999-23277 19990119; US 6042994 A Provisional US 1998-71977P 19980120, Provisional US 1998-71978P 19980120, US 1999-227734 19990108; EP 1050075 A1 EP 1999-903196 19990119, WO 1999-US1119 19990119; KR 2001024873 A KR 2000-707967 20000720; TW 466636 A TW 1999-100851 19990430

FDT AU 9923277 A Based on WO 9936953; EP 1050075 A1 Based on WO 9936953

PRAI US 1999-227734 19990107; US 1998-71977P 19980120; US 1998-71978P 19980120

AB WO 9936953 A UPAB: 19990908

NOVELTY - A nanoporous dielectric polymer coating on a substrate is optionally treated with a surface modifier, optionally heated to evaporate solvents, exposed to electron beam radiation and optionally thermally annealed to give a coating of low dielectric constant.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following: (a) a coated substrate formed as above; and (b) a semiconductor device produced by a process as above.

USE - As a nanoporous low dielectric constant silica film for semiconductor devices (claimed).

ADVANTAGE - Water content and dielectric constant are both lower than in thermally cured films, and mechanical strength and resistance to solvents and **oxygen plasma** are higher.

DESCRIPTION OF DRAWING(S) - An FTIR spectrum of various cured **wafers** is shown.

Dwg.1/1

L115 ANSWER 9 OF 25 WPIX (C) 2003 THOMSON DERWENT

AN 1999-419186 [35] WPIX

CR 2002-507624 [54]; 2002-658143 [70]; 2002-698898 [75]; 2003-018960 [01]

DNN N1999-312876 DNC C1999-123293

TI Micro-electromechanically tunable surface emitting laser and Fabry-Perot filter.

DC A85 L03 P81 U12 V07 V08

IN AZIMI, M; TAYEBATI, P; VAKHSHOORI, D; WANG, P

PA (CORE-N) CORETEK INC; (AZIM-I) AZIMI M; (TAYE-I) TAYEBATI P; (VAKH-I) VAKHSHOORI D; (WANG-I) WANG P

CYC 84

PI WO 9934484 A2 19990708 (199935)* EN 74p
RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW
W: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW
AU 9920174 A 19990719 (199951)
EP 1053574 A2 20001122 (200061) EN
R: DE FR GB IT
CN 1285034 A 20010221 (200131)
JP 2002500446 W 20020108 (200206) 57p
US 2002031155 A1 20020314 (200222)
US 6438149 B1 20020820 (200257)
US 2003012231 A1 20030116 (200308)

ADT WO 9934484 A2 WO 1998-US27681 19981228; AU 9920174 A AU 1999-20174 19981228; EP 1053574 A2 EP 1998-964965 19981228, WO 1998-US27681 19981228; CN 1285034 A CN 1998-813831 19981228; JP 2002500446 W WO 1998-US27681 19981228, JP 2000-527004 19981228; US 2002031155 A1 US 1998-105399 19980626; US 6438149 B1 US 1998-105399 19980626; US 2003012231 A1 Cont of US 1998-105399 19980626, US 2002-136057 20020429

FDT AU 9920174 A Based on WO 9934484; EP 1053574 A2 Based on WO 9934484; JP 2002500446 W Based on WO 9934484; US 2003012231 A1 Cont of US 6438149

PRAI US 1998-105399 19980626; US 1997-68931P 19971229; US 2002-136057 20020429

AB WO 9934484 A UPAB: 20030204

NOVELTY - Micro-electromechanically tunable surface emitting laser and Fabry-Perot filter have precise lateral and vertical dimension control and use preselected strain introduced into the quantum well structure to optimize gain performance.

DETAILED DESCRIPTION - A preselected amount and type of strain is

introduced into the quantum wells of a pre-grown crystalline semiconductor by depositing at least one thin film onto the upper surface of the member comprising the quantum wells, the thin film having an amount and type of strain opposite to that required in the member.

INDEPENDENT CLAIMS are included for the following: (a) a micromechanically tunable vertical cavity surface emitting laser (VCSEL) and Fabry-Perot filter having precise lateral and vertical dimension control. Controlled strain in the quantum well structure of the devices is used to provide optimized gain performance; (b) methods for fabrication of the VCSEL and filter.

USE - As wavelength tunable surface emitting semiconductor lasers and filters used in opto-electronics.

ADVANTAGE - The devices have precise dimensional control and have controlled strain in the quantum well regions so that gain properties are optimized.

DESCRIPTION OF DRAWING(S) - The drawing shows a micro-electromechanical tunable filter of the invention with a confocal cavity. Dwg.1/7

L115 ANSWER 10 OF 25 WPIX (C) 2003 THOMSON DERWENT
AN 1998-583619 [49] WPIX
DNN N1998-454642 DNC C1998-174668
TI Production of poly(hydrido-siloxane) copolymer used in films for planarising dielectric layers - comprises charging reaction vessel with at least one alkoxy-silane and aprotic solvent, adding acid mixture and polymerising.
DC A26 A85 G02 L03 U11
IN LEUNG, R Y; NAKANO, T
PA (ALLC) ALLIED-SIGNAL INC
CYC 26
PI WO 9847943 A1 19981029 (199849)* EN 36p
RW: AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE
W: CA CN IL JP KR RU SG
US 6015457 A 20000118 (200011)
TW 419493 A 20010121 (200138)
ADT WO 9847943 A1 WO 1998-US6165 19980330; US 6015457 A Provisional US 1997-44478P 19970421, US 1998-39289 19980312; TW 419493 A TW 1998-105463 19980410
PRAI US 1998-39289 19980312; US 1997-44478P 19970421
AB WO 9847943 A UPAB: 19981217
A process for producing a poly(hydrido-siloxane) copolymer of formula (I) comprises: (i) charging a reaction vessel with at least one alkoxysilane and an aprotic solvent, giving a first mixture; (ii) adding an acid mixture to provide a second reaction mixture; and (iii) polymerising the second reaction mixture.

(HSiO1.5)a(HSiO(OR))b(SiO2)c (I)

R = a mixture of H and 1-4C alkyl group; and a+b+c = 1; where $0.5 < a < 0.99$; $0.01 < b < 0.5$; and $0 < c < 0.5$.

Also claimed are: (1) a solution for coating a semiconductor device comprising the above and a solvent selected from dialkyl-ketals, alkyl-acetates, dialkyl-acetals, ethers, dialkyl **glycol** ethers and/or esters; (2) a process for producing the solution comprising: (i) charging a reaction vessel with a solution of poly(hidrido-siloxane) copolymer; (ii) removing alcohol and water from th poly(hydrido-siloxane) copolymer solution; and (iii) optionally diluting to desired copolymer concentration with a solvent; and (3) a semiconductor **integrated circuit** comprising a dielectric layer comprising the above copolymer, disposed overlaying a surface.

USE - The copolymer is used in films useful as planarising dielectric layers.

ADVANTAGE - The obtained layers have good resistance to degradation

by exposure to **oxygen plasma**.
Dwg.0/1

L115 ANSWER 11 OF 25 WPIX (C) 2003 THOMSON DERWENT
AN 1997-167067 [16] WPIX
DNN N1997-137362 DNC C1997-054122
TI Low temp. and pressure, direct bonding of nitride surface - by bonding using hydrogen atoms terminating surface dangling bonds.
DC L02 L03 U11
IN KURAHASHI, T; NAGAKUBO, M; SUZUKI, H
PA (NPDE) NIPPONDENSO CO LTD
CYC 3
PI DE 19637162 A1 19970313 (199716)* 10p
JP 09082588 A 19970328 (199723) 6p
US 5904860 A 19990518 (199927)
ADT DE 19637162 A1 DE 1996-19637162 19960912; JP 09082588 A JP 1995-260895 19950912; US 5904860 A US 1996-713033 19960912
PRAI JP 1995-260895 19950912
AB DE 19637162 A UPAB: 19970417
Direct bonding of the nitride surface of a first body (13) to the surface of a second body (14) involves: (a) cleaning the surfaces of the bodies; (b) terminating the bonds of the nitrogen atoms at the surface of the first body (13) with hydrogen atoms; and (c) bonding the surfaces of the bodies using the bonds of the hydrogen atoms. Step (b) is carried out by chemical etching with dil. hydrofluoric acid or by using a **hydrogen plasma** (36), produced by electron cyclotron resonance or by a radical beam source in vacuum.
USE - For direct bonding of a first component, covered with or made of nitride, to a second component, covered with or made of nitride or oxide or made of metal, semiconductor material, ceramic, **polymeric** material or the like, e.g. for bonding a base to an **IC chip** or sensor having a Si3N4 or TiN surface protective film or for bonding a base to a hard component (e.g. a precision tool tip), heat resistant component etc.
ADVANTAGE - The process provides solid, reliable and precise direct bonding of the bodies without the use of high temp. or high pressure so that deformation or cracks are not produced.
Dwg.2/6

L115 ANSWER 12 OF 25 WPIX (C) 2003 THOMSON DERWENT
AN 1996-193897 [20] WPIX
DNN N1996-162510
TI High-speed ashing method for semiconductor mfr. - by infiltrating **methanol** to resist pattern before ashing resist pattern using low-temperature plasma.
DC U11
PA (HITA) HITACHI LTD
CYC 1
PI JP 08064577 A 19960308 (199620)* 3p
ADT JP 08064577 A JP 1994-195029 19940819
PRAI JP 1994-195029 19940819
AB JP 08064577 A UPAB: 19960520
The method involves infiltrating **methanol** to a resist pattern formed on a semiconductor **wafer**.
An ashing processing is performed to the resist pattern using a low-temperature plasma, such as **hydrogen plasma**.
USE/ADVANTAGE - For ashing resist pattern formed on semiconductor **wafer**. Obtains high ashing rate even if only oxygen gas is used for ashing and even at low temperature.
Dwg.1/2

L115 ANSWER 13 OF 25 WPIX (C) 2003 THOMSON DERWENT
AN 1994-153989 [19] WPIX
DNN N1994-120968 DNC C1994-070626
TI Phenolic hydroxyl gp.-contg. resin for dry development using plasma etching - forms good resist pattern at low temp. and includes sulphuric acid ester component.
DC A89 E19 G06 L03 P84 U11
PA (JAPS) NIPPON GOSEI GOMU KK
CYC 1
PI JP 06095376 A 19940408 (199419)* 10p
JP 3127612 B2 20010129 (200113) 10p
ADT JP 06095376 A JP 1992-270750 19920916; JP 3127612 B2 JP 1992-270750 19920916
FDT JP 3127612 B2 Previous Publ. JP 06095376
PRAI JP 1992-270750 19920916
AB JP 06095376 A UPAB: 19940627
The compsn. comprises resin, contg. phenol-type hydroxyl gp., and at least one cpd. of formula R1-NH-R2 (1), and further contg. 1,2-quinone-diazide sulphonic acid ester component. In (1), R1 and R2 = H, -SO2-R3, -CO-R4 (R3, R4 = alkyl or aryl gp. opt. substd. with at least one halogen atom, alkyl, alkoxy, nitro or CN gp.) or they may combine to form a ring with N atom, where one of R1 and R2 is H and the other is -SO2-R3.

Suitable cpds. of formula (1) are maleimide, saccharin, N-benzoyl-4-toluenesulphonamide, di(4-toluenesulphonyl) amine and p-toluene-sulphonamide.

USE/ADVANTAGE - For the resist which can be developed by plasma etching after silylation after exposure, allowing silylation with hexamethyldisilazane (HMDS) at lower temp., to give resist pattern of good profile, with high sensitivity.

In an example, esterified novolak A is prepd. by reacting 100g of novolak, prepd. by condensing m-cresol (303g) and p-cresol (130g) with formaldehyde (37% aq. 276g) under the presence of oxalic acid, with 36.4g of 1,2-naphthoquinonediazide- 5-sulphonyl chloride in aq. propylene-**glycol** monomethylether acetate (PGMA) in the presence of triethylamine, followed by purificn. Resist compsn. (esterified novolak A 20g/ saccharin 2.0g/ 'NEOPENGELB' (dye) 0.6g/ 'KAYARAITO-B' (dye) 1g/ 'MEGAFAKKU-F172' (surfactant) 0.004g/) is dissolved in PGMA (58g) and filtered. The soln. is spin-coated on silicone **wafer** to give 1.5 micron dried thickness, exposed in a stepper and baked at a fixed temp. in vacuum for 3 mins. and then silylated with HMDS vapour at the same temp. for 2 mins. The silylated **wafer** undergoes anisotropic **oxygen plasma** etching in an ion-etching appts. with magnetron enhancement.

The samples with saccharin, p-toluenesulphonamide (1.0g) or maleimide (2.0g) showed good pattern formation with silylation temp. of 140 deg.C, while control sample without cpds. of formula (1) could not form pattern at the same temp. and gave poor pattern at 180 deg.C.
Dwg.0/0

L115 ANSWER 14 OF 25 WPIX (C) 2003 THOMSON DERWENT
AN 1994-064842 [08] WPIX
CR 1996-286356 [29]
DNN N1994-050857 DNC C1994-029054
TI Thin film substrate through-hole metallisation used in mfr. of thin film semiconductor **chip** carrier - has **chip** mounted on one major surface of carrier and electrically connected to ground plane via through holes.
DC A35 L03 M13 P73 U11 U14
IN BLACKWELL, K J; CHEN, P C; DELIMAN, S E; KNOLL, A R; MATARESE, G J; WEALE, R D
PA (IBMC) INT BUSINESS MACHINES CORP

CYC 1
PI US 5288541 A 19940222 (199408)* 10p
ADT US 5288541 A US 1991-779411 19911017
PRAI US 1991-779411 19911017
AB US 5288541 A UPAB: 19960731
The thin film **chip** carrier comprises a thin film **polymeric** substrate (10) of, e.g. a **polyimide** such as 'KAPTON' (RTM) of a thickness ranging from 12.5 to 125 microns. Pref. the upper surface (15) is subjected to an **oxygen plasma**, followed by a thin seed layer (30) of chromium (20) and copper (25), deposited by magnetron **sputtering**. this layer is patterned into lands encircling through holes and circuit lines. Holes (50) are now drilled through the substrate (40), which is now fed in roll format into a roll **sputter** coating appts. (60) containing a chilled drawn for dissipating heat generated by the coating process.
USE/ADVANTAGE - For use as a semiconductor **chip** carrier. Enables thin film devices to be metallised having through holes in substantially correct locations.
Dwg.1d/3
Dwg.1d/3

L115 ANSWER 15 OF 25 WPIX (C) 2003 THOMSON DERWENT
AN 1992-274130 [33] WPIX
TI Pattern forming for thin film magnet heat - by forming resist pattern on substrate, eliminating processing material from area uncovered by result pattern, by dry etching, then evaporating polymerisation to give uniform film.
DC A89 G06 L03 T03 V02
PA (HITA) HITACHI LTD
CYC 1
PI JP 04187786 A 19920706 (199233)* 6p
ADT JP 04187786 A JP 1990-314043 19901121
PRAI JP 1990-314043 19901121
AB JP 04187786 A UPAB: 19931006
Pattern forming comprises: forming resist pattern on substrate having large height difference on the surface within the processing area; eliminating processing material from the area uncovered with the resist pattern by dry etching.
The resist is formed by evaporative polymerisation to produce a uniform resist film thickness. Patterning of the substrate having height difference on the surface pref. consists of first layer removable by **oxygen plasma**. The second layer is formed on the first layer and is unremovable by **oxygen plasma**. The third layer is formed by evaporative polymerisation and is patternable by irradiation of electromagnetic wave or of particle, and by development.
USE/ADVANTAGE - For fine processing in lithography technology to accurately process thin film on a substrate having a large difference of height on the surface. The film has uniform thickness, even the concave section exists on the surface which prevents re-deposition during the ion-trimming process.
In an example, on a silicon **wafer** having line and space strips pattern (10 micron depth, 50 micron width) of **polyimide** resin, Permalloy film was formed at 1 micron of thickness by **sputtering**. Then the **polyimide** film (2 micron thick) having general fomula (I) was formed on the pattern by evaporative polymerisation. After heat treating at 100 deg.C, the film was covered with a photomask having stripe pattern of line and space (5 micron width) at a right angle to the **polyimide** pattern, and was irradiated by far ultraviolet light of 254 nm (400 mJ/cm2). Development was carried in N,N-dimethylformamide. The positive-resist pattern was formed to expose Permalloy. The exposed Permalloy was etched by Ar ion trimmingin 1

L115 ANSWER 16 OF 25 WPIX (C) 2003 THOMSON DERWENT
AN 1992-272893 [33] WPIX
DNN N1992-208779 DNC C1992-121267
TI Electro-insulation films for semiconductor devices - obtd. coating a protective coat of poly silicon on insulation film contg. organic gps. giving good **oxygen plasma** resistance and planarisation ability.
DC A26 A82 A85 G02 L03 U11
PA (FUIT) FUJITSU LTD
CYC 1
PI JP 04185639 A 19920702 (199233)* 4p
ADT JP 04185639 A JP 1990-314570 19901120
PRAI JP 1990-314570 19901120
AB JP 04185639 A UPAB: 19931025
Mfr. involves forming a protective coat of a silicone polymer of formula (SiO4/2)l(PO5/2)m(BO3/2)n (I) on an electro-insulation film contg. organic gps.. In (I), l is 70-100; m is 15-0; and n is 15-0.

Also claimed are semiconductor devices with a protective coat with a planarised surface on an electro-insulation film bearing organic gps. covering a wiring pattern.

USE/ADVANTAGE - The films with the protective coats on multilayered wiring of semiconductor **IC**'s have excellent O2 plasma resistance and substrate surface planarisation ability and are useful for mfg. highly integrated LSI's and VLSI's with high reliability. The protective coats can be applied by spin coating.

In an example, into a soln. of 132g tetraacetoxysilane in 500ml tetrahydroxyfuran, was added 73g triethylboric acid. The mixt. was refluxed for 3 hrs. and from the mixt., was distilled off tetrahydrofuran to give an ester-interchanged prod.. To the prod., was added 30ml **methanol**. The mixt. was stirred for 30 mins. at room temp.. Into the mixt. was dropped 20ml ion-exchanged water. The mixt. was heated for 3 hrs. at 50 deg.C to hydrolyse and polycondense. From the reaction mixt., were removed **methanol** and water to give a resin with a mean mol.wt. of 1.2x10 power (3) and the resin was dissolved into butyl cellosolve to give a resin soln.. On an Al-wired Si substrate, was applied methylsilsesquioxane resin in a thickness of 0.8 microns by spin-coating, the substrate was heat treated for 30 secs. at 250 deg.C. Onto the methyl ladder silicon resin film, was applied the resin soln. in a thickness of 0.5 microns by spin coating and the substrate was dried for 30 mins. at 150 deg.C and heat treated for 30 mins. at 250 deg.C to give a wired layer having a planarised surface with a difference of below 0.
Dwg.0/0

L115 ANSWER 17 OF 25 WPIX (C) 2003 THOMSON DERWENT
AN 1992-218525 [27] WPIX
DNN N1992-165941 DNC C1992-098906
TI Sub-micron photolithographic structurising using dry resist - based on polymer with carboxylic anhydride and tert. butyl carboxylate gps..
DC A89 G07 L03 P84 U11
IN AHNE, H; BIRKLE, S; BORNDOERFER, H; LEUSCHNER, R; SEBALD, M; SEZI, R
PA (SIEI) SIEMENS AG
CYC 12
PI EP 492256 A1 19920701 (199227)* DE 9p
R: BE CH DE ES FR GB IT LI NL SE
JP 05011457 A 19930122 (199308) 8p
US 5384220 A 19950124 (199510) 7p
EP 492256 B1 19960814 (199637) DE 9p
R: BE CH DE ES FR GB IT LI NL SE
DE 59108083 G 19960919 (199643)

ES 2090218 T3 19961016 (199647)
JP 3290195 B2 20020610 (200241) 7p
ADT EP 492256 A1 EP 1991-121088 19911209; JP 05011457 A JP 1991-353048 19911218; US 5384220 A US 1991-811706 19911220; EP 492256 B1 EP 1991-121088 19911209; DE 59108083 G DE 1991-508083 19911209, EP 1991-121088 19911209; ES 2090218 T3 EP 1991-121088 19911209; JP 3290195 B2 JP 1991-353048 19911218
FDT DE 59108083 G Based on EP 492256; ES 2090218 T3 Based on EP 492256; JP 3290195 B2 Previous Publ. JP 05011457
PRAI DE 1990-4041002 19901220
AB EP 492256 A UPAB: 19931006
Sub-micron photolithographic structurisation is carried out by (a) giving a substrate a photoresist coating of a polymer (I) contg. carboxylic anhydride and tert.-butyl carboxylate gps., a photoinitiator (II) releasing an acid on exposure and a suitable solvent; (b) drying the coating; (c) selective exposure; (d) heat treatment so that the exposed areas become hydrophilic; (e) liquid silylation; and (f) dry development in an anisotropic **oxygen plasma**.

(I) pref. contains anhydride gps. derived from maleic anhydride and tert.-butyl carboxylate gps. derived from tert.-butyl (meth)acrylate or vinylbenzoate. (I) pref. is a copolymer of maleic anhydride and tert.-butyl (meth)-acrylate or vinylbenzoate. (II) is an onium cpd. Stage (d) is carried out for 15-200s at 80-140 deg.C; and (e) with an apolar, aprotic silylation soln., pref. of an aminosiloxane in an organic solvents, esp. anisole, dibutyl ether and/or diethylene **glycol** dimethyl ether, or with a polar protic silylation soln., pref. of an aminosiloxane in a mixt. of water and alcohol, esp. EtOH and/or i-PrOH.

USE/ADVANTAGE - For structurising Si **wafers**. Gives structures with high resolution (sub half micron range) with steel sides and is suitable for top surface imaging (TSI) systems for dry development. Processing is simple and the resist has high etching resistance and high sensitivity (under 20 mJ/cm2), esp. in the deep UV region. Metallisation (silylation) can be carried out in standard appts. under normal conditions (room temp. and normal pressure)
0/0

L115 ANSWER 18 OF 25 WPIX (C) 2003 THOMSON DERWENT
AN 1992-017663 [03] WPIX
DNN N1992-013408 DNC C1992-007620
TI Resist material - comprises polysiloxane, obtd. by hydrolysing alkoxy-silane having oxirane ring then condensing and dehydrating and acid generator.
DC A26 A89 E19 G06 L03 P84 U11
IN BAN, H; KAWAI, Y; KIMURA, T; NAKAMURA, J; TANAKA, A
PA (NITE) NIPPON TELEGRAPH & TELEPHONE CORP
CYC 6
PI EP 466025 A 19920115 (199203)* 48p
R: DE FR GB
JP 04338958 A 19921126 (199302) 21p
EP 466025 A3 19920902 (199338) 48p
US 5457003 A 19951010 (199546) 34p
KR 9407795 B1 19940825 (199623)
EP 466025 B1 19990310 (199914) EN
R: DE FR GB
DE 69130966 E 19990415 (199921)
ADT EP 466025 A EP 1991-111109 19910704; JP 04338958 A JP 1991-138060 19910610; EP 466025 A3 EP 1991-111109 19910704; US 5457003 A CIP of US 1991-724115 19910701, US 1993-99398 19930730; KR 9407795 B1 KR 1991-11370 19910705; EP 466025 B1 EP 1991-111109 19910704; DE 69130966 E DE 1991-630966 19910704, EP 1991-111109 19910704
FDT DE 69130966 E Based on EP 466025

PRAI JP 1990-177257 19900706; JP 1990-320781 19901127
AB EP 466025 A UPAB: 19931123
A resist material comprising: (a) a polysiloxane having partial structural units of formulae (1) to (3); where R1, R2 and R3 = an organic gp. part or all of the gps. R1-R3 have an oxirane ring, and the partial structural units (1)-(3) are connected to each other so as to complete siloxane bonds; and (b) an acid generator.
Also claimed are: (i) prodn. of the resist material and ii) formation of resist patterns.
USE/ADVANTAGE - The resist material is for use in lithography e.g. in the prodn. of **integrated circuits** and in two layer resists. The material can reproduce negative patterns with high accuracy and has high resistance to **oxygen plasma** etching (high O2R1E resistance). @(48pp Dwg.No.1/6)
1/6

L115 ANSWER 19 OF 25 WPIX (C) 2003 THOMSON DERWENT
AN 1991-009584 [02] WPIX
DNN N1991-007498 DNC C1991-004203
TI Collimated metal deposition - using dual overhang structure to eliminate excess metal deposition.
DC A85 L03 P73 P84 U11
IN MATHAD, G W; STANASOLOV, D; VIA, G G; MATHAD, G S; STANASOLOVICH, D
PA (IBMC) IBM CORP; (IBMC) INT BUSINESS MACHINES CORP
CYC 5
PI EP 406544 A 19910109 (199102)*
R: DE FR GB
JP 03046330 A 19910227 (199115)
US 5024896 A 19910618 (199127)
US 5258264 A 19931102 (199345) 5p
EP 406544 B1 19941228 (199505) EN 6p
R: DE FR GB
DE 69015472 E 19950209 (199511)
ADT EP 406544 A EP 1990-108998 19900512; JP 03046330 A JP 1990-177643 19900706; US 5024896 A US 1989-350182 19890706; US 5258264 A Div ex US 1989-350182 19890706, Cont of US 1991-665372 19910306, US 1992-926659 19920806; EP 406544 B1 EP 1990-108998 19900512; DE 69015472 E DE 1990-615472 19900512, EP 1990-108998 19900512
FDT US 5258264 A Div ex US 5024896; DE 69015472 E Based on EP 406544
PRAI US 1989-350182 19890706
AB EP 406544 A UPAB: 19930928
A structure for depositing metal comprises: a first lift-off layer (I) deposited on a substrate; a first barrier layer (II) deposited on (I) and having different etch properties; a second lift-off layer (III) deposited on (II) and having similar etch properties to (I); a second barrier layer (IV) deposited on (III) and having similar etch properties to (II). Pref. (i) lift-off layers (I, III) are etchable in O2 or O2 contg. plasma, e.g. **polyimide**, (ii) barrier layers (II, IV) are etchable in a plasma of gas selected from CF4, C2F6 or CHF3 with or without O2 as an additive, e.g. HMDS, SiO2, Si3N4, resin glass.
Further disclosed is a structure shaped to provide an opening with 2 overhangs in the barrier layers. Upon deposition of metal, metal atoms are screened by the first overhang and aligned by the second overhang thus representing the equivalent of a light-beam collimator.
USE/ADVANTAGE - Improved metal lift--off process in which undesired footing is eliminated even when narrow lines and spacing are defined. useful for a dual overhang, collimated metal process for deposting metal lines on a semiconductor **chip**.
In an example, a semiconductor **wafer** (10) with I.C.'s formed is coated with **polyimide** layer (12). Barrier layer (14) of plasma polymerised HMDS is deposited on **polyimide**, 2000

Angstroms thick. Second lift-off layer (16) identical to first lift-off layer (12) is formed on HMDS layer (14). Second barrier layer (18) similar to layer (14) deposited on second lift-off layer (16). Photoresist (20) applied and patterned. @(5pp Dwg.No.1C/1)@

L115 ANSWER 20 OF 25 WPIX (C) 2003 THOMSON DERWENT
AN 1989-150249 [20] WPIX
DNN N1989-114800 DNC C1989-066526
TI Mfg. semiconductor device with silicon glass passivating layers - by coating, pref. by spinning, with precursor layer obtd. from lower alcohol and silicon (IV) anhydride and curing to form dielectric layer.
DC A89 G06 L01 L03 P42
IN RYAN, V W; SMOLINSKY, G
PA (AMTT) AMERICAN TELEPHONE & TELEGRAPH CO
CYC 1
PI US 4826709 A 19890502 (198920)* 8p
ADT US 4826709 A US 1988-161876 19880229
PRAI US 1988-161876 19880229
AB US 4826709 A UPAB: 19930923
A process for producing a silica glass passivating layer on a device comprises coating a precursor layer on a non-planar substrate, curing it to give the silica dielectric layer and continuing the fabrication of the device. The precursor layer material is produced by reacting a lower alcohol (not **methanol**) with a Si(IV) anhydride composed of lower organic acid moieties bound to Si.

USE/ADVANTAGE - The process produces long shelf-life sols. which are easily spun onto substrates and cured to form layers with low dielectric constants, high breakdown voltages and low mechanical stresses. They do not outgas below 900 deg.C, are resistant to wet etchants and to **O -plasmas**. They are especially suitable for multilevel resist applications and useful for **IC** devices in general.
0/4

L115 ANSWER 21 OF 25 WPIX (C) 2003 THOMSON DERWENT
AN 1988-135908 [20] WPIX
DNN N1988-103515 DNC C1988-060652
TI Pattern-forming material - comprises tri methyl-silyl-methyl-methacrylate iso-propylene-oxy-tri-methyl-silane copolymer.
DC A14 A89 G06 L03 P83 U11
PA (FUIT) FUJITSU LTD
CYC 1
PI JP 63077053 A 19880407 (198820)* 3p
ADT JP 63077053 A JP 1986-220900 19860920
PRAI JP 1986-220900 19860920
AB JP 63077053 A UPAB: 19930923
Pattern-forming material consists of copolymer of (A) trimethylsilyl methylmethacrylate of formula (I) and (B) isopropenoxy trimethylsilane of formula (II). The copolymer pref. consists of 60-95 mol. % monomer (A) and 5-40 mol. % monomer (B) and has wt. average molecular wt., 10,000-500,000.

ADVANTAGE - The pattern-forming material has improved film-forming properties without inhibiting resolution, sensitivity and anti-**oxygen plasma** properties.

In an example, compsn. consisting of 15.5g trimethylsilyl methylmethacrylate, 1.3g isopropenoxy trimethylsilane, 0.4g azobisiso butylonitrile and 50cc benzene were reacted at 60 deg. C for 24 hr. The solid product was dissolved in benzene and deposited from **methanol**. The deposits were dissolved in benzene, and deposited from **methanol** again to obtain the required polymer.

The polymer had average molecular wt,, 15x10 power 4. The polymer was dissolved in cyclohexane in a concn. of 10 wt. % to obtain resist

soln. The resist soln. was applied on a silicone **wafer**. The surface of the coat film obtd. was observed by an electromicroscope to be uniform and smooth and was suitable as an upper resist of a double-layered resist. The resist has sensitivity of 6.3 microcurie/cm2 and resolution of 0.5 micron for line-and-space.
0/0

L115 ANSWER 22 OF 25 WPIX (C) 2003 THOMSON DERWENT
AN 1983-846322 [51] WPIX
DNN N1983-225656 DNC C1983-123510
TI Forming fine etched patterns in electronic device mfr. - using dry-etchable polymer masks and litho-sensitive silyl-contg. polymer resists.
DC A89 G06 L03 U11
IN SAIGO, K; SUZUKI, M
PA (NIDE) NEC CORP
CYC 9
PI EP 96596 A 19831221 (198351)* EN 58p
R: BE DE FR GB NL
JP 58214148 A 19831213 (198404)
JP 58215409 A 19831214 (198405)
JP 59015243 A 19840126 (198410)
JP 59015419 A 19840126 (198410)
JP 59084429 A 19840516 (198426)
US 4551417 A 19851105 (198547)
EP 96596 B 19860604 (198623) EN
R: BE DE FR GB NL
DE 3363914 G 19860710 (198629)
CA 1207216 A 19860708 (198632)
JP 01057333 B 19891205 (199001)
JP 03064861 B 19911008 (199144)
JP 03065545 B 19911014 (199145)
JP 05065527 B 19930917 (199340) 3p
EP 96596 B2 19940323 (199412) EN 22p
R: BE DE FR GB NL
ADT EP 96596 A EP 1983-303324 19830608; JP 58214148 A JP 1982-98089 19820608; JP 58215409 A JP 1983-98090 19830608; JP 59015243 A JP 1982-123865 19820716; JP 59015419 A JP 1982-123866 19820716; JP 59084429 A JP 1982-194286 19821105; US 4551417 A US 1983-501201 19830106; JP 03064861 B JP 1982-98090 19820608; JP 03065545 B JP 1982-123965 19820716; JP 05065527 B JP 1982-123866 19820716; EP 96596 B2 EP 1983-303324 19830608
FDT JP 05065527 B Based on JP 59015419
PRAI JP 1982-98089 19820608; JP 1982-98090 19820608; JP 1982-123865 19820716; JP 1982-123866 19820716; JP 1982-194286 19821105
AB EP 96596 A UPAB: 19930925
Formation of patterns in mfr. of electronic devices by (a) forming on an etchable substrate a dry-etchable organic polymer layer (I) and a **polymeric** resist film (II) which contains trialkylsilyl, dimethylphenylsilyl or trialkoxysilyl gps., (b) lithographically forming a required pattern in (II), dry-etching (I) using patterned (II) as a mask, and etching the substrate using unetched areas of (I) as a mask. Dry etching is esp. by reactive **sputter** using oxygen gas. Substd. silyl gps. in patterned resist film is at least 10 power 16/sq.cm.

Pref. (II) comprises (a) trialkylsilylstyrene, esp. trimethyl or triethyl-silylstyrene, homo- or copolymers, esp. with chloromethyl/styrene or glycidyl methacrylate; (b) trimethylallyl silane/diallyl phthalate or terephthalate copolymers; (c) a trimethylsilyl-substd. novolak; (d) 2-trimethylsiloxyethyl methacrylate homo- or copolymers, esp. with methyl methacrylate; (e) dimethylphenylsilylstyrene homo- or co-polymers; and (f) 3-trimethoxysilylpropyl methacrylate copolymers, esp. with glycidyl methacrylate. Unspecified monomers are free from substd. silyl gps.

The resists are durable to dry etching with **oxygen plasma** and display high sensitivity and resolution capabilities:polymer layer can be applied thickly to cover stepped substrate. Esp. useful in mfr. of LSI, bubble memory devices.
0/1

L115 ANSWER 23 OF 25 JAPIO COPYRIGHT 2003 JPO
AN 1996-064577 JAPIO
TI MANUFACTURE OF SEMICONDUCTOR
IN ISHIDA TAKASHI; MIYAMOTO HIROAKI
PA HITACHI LTD
PI JP 08064577 A 19960308 Heisei
AI JP 1994-195029 (JP06195029 Heisei) 19940819
PRAI JP 1994-195029 19940819
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1996
AB PURPOSE: To make it possible to obtain a large ashing rate even in a state that an RF power is small and the temperature of a **wafer** is low.
CONSTITUTION: A semiconductor manufacturing method is a method of performing an ashing on a resist patterned film 3 formed on a semiconductor **wafer** 1 with low-temperature plasma containing **oxygen plasma** as its main component. After a **methanol** is soaked into a resist before the asing, a plasma ashing is performed. The resist patterned film is formed on a metal film. The metal film consists of some one of a Cr film, a Cr oxide film and a Cr alloy film or a laminated film of Cr, Ni, Cu and Au films.
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L115 ANSWER 24 OF 25 JAPIO COPYRIGHT 2003 JPO
AN 1988-122224 JAPIO
TI THIN FILM HYBRID **INTEGRATED CIRCUIT**
IN OZAWA TAKEO
PA NEC CORP
PI JP 63122224 A 19880526 Showa
AI JP 1986-270145 (JP61270145 Showa) 19861112
PRAI JP 1986-270145 19861112
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1988
AB PURPOSE: To prevent the adhesion from deteriorating by restraining any water content from permeating into the gap between insulating layers of organic high molecular films and wiring conductors of metallic thin films for improving the reliability by a method wherein protective layers covering the peripheral parts of wiring conductors and the parts adjoining the peripheral parts are provided.
CONSTITUTION: A substrate 1 is coated with **polyimide** resin around 2 μm thick and then the **polyimide** resin is selectively removed by **oxygen plasma** etching process to form interlayer insulating layers 4. Next, a Ni-Cr thin film around 0.1 μm thick, a Pb thin film around 0.1 μm thick and an Au thin film around 0.8 μm thick are laminated by magnetron **sputtering** process to form a metallic thin film around 1 μm thick. Then the second wiring conductor 5 is formed. Finally protective layers 6 comprising epoxy resin are formed to cover the peripheral parts of the second wiring conductor 5 and the interlayer insulating layers 4 adjoining the peripheral parts.
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L115 ANSWER 25 OF 25 JAPIO COPYRIGHT 2003 JPO
AN 1985-194445 JAPIO
TI ACRYLIC POLYMER CONTAINING SILICON ATOM
IN SAIGO KAZUHIDE
PA NEC CORP
PI JP 60194445 A 19851002 Showa
AI JP 1984-49839 (JP59049839 Showa) 19840315

PRAI JP 1984-49839 19840315
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1985
AB PURPOSE: To obtain a polymer for a resist material having superior resistance to dry etching and suitable for use in the manufacture of an **integrated circuit** or the like by polymerizing a monomer mixture contg. trialkylsilylmethyl methacrylate as a constituent unit.
CONSTITUTION: A copolymer represented by the formula (where A is a repeating unit from an ethylenic unsatd. compound, R is lower alkyl, and X and Y are the mole fractions of the constituent units) is manufactured by polymerizing a mixture of trialkylsilylmethyl methacrylate with a monomer A such as (meth)acrylic ester, a styrene deriv. or divinylbenzene in an org. solvent. Only the monomer mixture may be polymerized. The resulting polymer soln. or molten polymer is put in a solvent which does not dissolve the polymer such as **methanol** or hexane, and a white powdery polymer is taken out by filtration and vacuum-dried. When the purified polymer is used, a resist film having high resistance to dry etching with **oxygen plasma** or the like can be formed.
The resist film is suitable for the accurate formation of a fine pattern for manufacturing an **integrated circuit** or a bubble memory element.

L116 ANSWER 1 OF 12 WPIX (C) 2003 THOMSON DERWENT
AN 2002-270654 [32] WPIX
DNN N2002-210634
TI Purge gas assembly in chemical vapor deposition processing chamber, has grooves in deflector, which directs purge gas at an angle relative to radial line from central axis of deflector.
DC U11 V05
IN GILLIAM, A; KELKAR, U; KHURANA, N; MOSELY, R C; POPIOLKOWSKI, A; SHERSTINSKY, S; SMITH, P F; YOSHIDOME, T; YUDOVSKY, J; ZUNIGA, L A; KELKAR, U M; MOSELY, R; **SMITH, P**
PA (MATE-N) APPLIED MATERIALS INC
CYC 30
PI EP 1137042 A2 20010926 (200232)* EN 17p
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR
JP 2001297991 A 20011026 (200232) 38p
KR 2001083246 A 20010831 (200232)
US 6350320 B1 20020226 (200232)
TW 489333 A 20020601 (200319)
ADT EP 1137042 A2 EP 2001-301623 20010222; JP 2001297991 A JP 2001-46653 20010222; KR 2001083246 A KR 2001-9057 20010222; US 6350320 B1 US 2000-510110 20000222; TW 489333 A TW 2001-103851 20010220
PRAI US 2000-510110 20000222
AB EP 1137042 A UPAB: 20020521
NOVELTY - A ring-shaped deflector (76) has deflection surface (90) with grooves (100) which directs the flow of a purge gas at an angle relative to a radial line (104) from a central axis of the deflector over the deflection surface. An edge ring with an inner annular lip, is provided on a portion of an upper surface of the deflector such that the edge ring and deflector forms a purge gas passage way.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(a) Substrate processing apparatus;
(b) Gas delivering method to substrate
USE - In chemical vapor deposition (CVD), physical vapor deposition (PVD) and etching apparatuses for delivering gas to edge of semiconductor substrate for fabrication of **integrated circuits**.
ADVANTAGE - Ensures uniform purge gas flow to the substrate and reduces the pressure differential effects to achieve higher degree of depostion uniformity on the substrate. Prevents unwanted depostion of purge gas such as argon on the edge and back side of the substrate.
DESCRIPTION OF DRAWING(S) - The figure shows a top view of the deflector with angled grooves.
Ring-shaped deflector 76
Deflection surface 90
Grooves 100
Radial line 104
Dwg.6, 7/8

L116 ANSWER 2 OF 12 WPIX (C) 2003 THOMSON DERWENT
AN 2001-521305 [57] WPIX
CR 2001-257355 [26]; 2001-521304 [57]
DNN N2001-386225
TI Cryptography acceleration **chip** has classification engine that receives complete IP packet and determines specific keys needed to encrypt or decrypt packet.
DC T01 W01
IN KRISHNA, S; LAW, P; LIN, D; OWEN, C; **SMITH, P**; TARDO, J; LIN, D C; SMITH, P N; TARDO, J J
PA (BROA-N) BROADCOM CORP

CYC 95
PI WO 2001005087 A2 20010118 (200157)* EN 45p
RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TZ UG ZW
W: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
AU 2000063425 A 20010130 (200157)
EP 1192782 A2 20020403 (200230) EN
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI
US 2003023846 A1 20030130 (200311)
ADT WO 2001005087 A2 WO 2000-US18617 20000707; AU 2000063425 A AU 2000-63425 20000707; EP 1192782 A2 EP 2000-950302 20000707, WO 2000-US18617 20000707; US 2003023846 A1 Provisional US 1999-142870P 19990708, Provisional US 1999-159011P 19991012, Cont of US 2000-610722 20000706, US 2002-218206 20020812
FDT AU 2000063425 A Based on WO 200105087; EP 1192782 A2 Based on WO 200105087
PRAI US 1999-159011P 19991012; US 1999-142870P 19990708; US 2000-610722 20000706; US 2002-218206 20020812
AB WO 200105087 A UPAB: 20030214
NOVELTY - The cryptography acceleration **chip** has a classification engine (204) configured to receive a complete IP packet and determines what keys are needed to encrypt or decrypt the packet.
DETAILED DESCRIPTION - The cryptography acceleration **chip** has a classification engine (204) which determines the keys by parsing fields in a header of the IP packet to determine a flow to which the packet belongs. The flow has one or more associated keys for encrypting or decrypting the packet. The engine supports all necessary modes for IPSec security processing. The **chip** includes internal and external local memories and hash-based look-up table.
USE - For use in cryptography, also incorporated on network line cards or service modules and used in applications as diverse as connecting a single computer to WAN, to large corporate networks, to networks servicing wide geographic areas.
ADVANTAGE - Implements IPSec specification at much faster rates than are achievable with current **chip** designs. Has much reduced local memory requirements.
DESCRIPTION OF DRAWING(S) - The figure shows the high level diagram of cryptography acceleration **chip**.
Classification engine 204
Dwg.2/7

L116 ANSWER 3 OF 12 WPIX (C) 2003 THOMSON DERWENT
AN 2001-257355 [26] WPIX
CR 2001-521304 [57]; 2001-521305 [57]
DNN N2001-183587
TI Cryptography acceleration method involves splitting incoming data packet into multiple fixed size cells and processing a fixed size cell.
DC W01
IN KRISHNA, S; LAW, P; LIN, D; OWEN, C; TARDO, J; **SMITH, P**; LIN, D C; TARDO, J J
PA (BROA-N) BROADCOM CORP
CYC 95
PI WO 2001005089 A2 20010118 (200126)* EN 38p
RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TZ UG ZW
W: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE

SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
AU 2000070514 A 20010130 (200127)
EP 1192781 A2 20020403 (200230) EN
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI
EP 1192782 A2 20020403 (200230) EN
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI
EP 1192783 A2 20020403 (200230) EN
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI
US 6477646 B1 20021105 (200276)
US 2002199101 A1 20021226 (200304)
US 2003014627 A1 20030116 (200308)

ADT WO 2001005089 A2 WO 2000-US18545 20000707; AU 2000070514 A AU 2000-70514 20000707; EP 1192781 A2 EP 2000-950299 20000707, WO 2000-US18537 20000707; EP 1192782 A2 EP 2000-950302 20000707, WO 2000-US18617 20000707; EP 1192783 A2 EP 2000-959143 20000707, WO 2000-US18545 20000707; US 6477646 B1 Provisional US 1999-142870P 19990708, Provisional US 1999-159012P 19991012, US 2000-510486 20000223; US 2002199101 A1 Provisional US 1999-142870P 19990708, Provisional US 1999-159012P 19991012, Cont of US 2000-510486 20000223, US 2002-227491 20020823; US 2003014627 A1 Provisional US 1999-142870P 19990708, Provisional US 1999-159012P 19991012, Cont of US 2000-610798 20000706, US 2002-218159 20020812

FDT AU 2000070514 A Based on WO 200105089; EP 1192781 A2 Based on WO 200105086; EP 1192782 A2 Based on WO 200105087; EP 1192783 A2 Based on WO 200105089; US 2002199101 A1 Cont of US 6477646

PRAI US 2000-510486 20000223; US 1999-142870P 19990708; US 1999-159012P 19991012; US 1999-159011P 19991012; US 2002-227491 20020823; US 2000-610798 20000706; US 2002-218159 20020812

AB WO 200105089 A UPAB: 20030204
NOVELTY - The incoming IP packet is split into multiple fixed size cells if it is larger than single fixed size cell, else the packet is converted into single fixed size cell. The fixed size cell is processed and then recombined into a processed IP packet. The processed IP packet is stored in system memory.

DETAILED DESCRIPTION - Processing of fixed size cell obtained by splitting incoming IP packet, involves performing encryption-decryption and authentication-digital signature processing. INDEPENDENT CLAIMS are also included for the following:

(a) Cryptography acceleration **chip**;

(b) Method for sequencing fixed size cells in cryptography acceleration **chip**

USE - For accelerating cryptography processing of IP packets, in router, gateway of network.

ADVANTAGE - Allows to fetch and process cells in predictable time frame, as pipeline has known throughput and timing characteristics. Local memory is not required to store packet data and control parameters, hence implementation cost is reduced. Overall performance is improved, since both encryption-decryption and authentication-digital signature processing are ensured.

DESCRIPTION OF DRAWING(S) - The figure shows block diagram of cryptography acceleration **chip**.

Dwg.4/8

L116 ANSWER 4 OF 12 WPIX (C) 2003 THOMSON DERWENT
AN 2000-317526 [27] WPIX
DNN N2000-238334 DNC C2000-096044
TI An anti-falsification paper useful for making falsification of an object very difficult has anti-falsification elements with photoluminescent segments exhibiting linearly polarized luminescence.

DC A12 A97 F09 P76 P85
IN **SMITH, P**; WEDER, C
PA (ETHZ-N) ETHZ INST POLYMERE; (LAND-N) LANDQART
CYC 90
PI WO 2000019016 A1 20000406 (200027)* DE 35p
RW: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SL SZ TZ UG ZW
W: AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US UZ VN YU ZA ZW
AU 9956150 A 20000417 (200035)
BR 9914061 A 20010619 (200140)
EP 1115949 A1 20010718 (200142) DE
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI
EP 1233106 A1 20020821 (200262) DE
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI
AU 754452 B 20021114 (200303)
EP 1115949 B1 20030102 (200310) DE
R: AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU MC NL PT RO SE SI
DE 59903926 G 20030206 (200318)
ADT WO 2000019016 A1 WO 1999-CH450 19990922; AU 9956150 A AU 1999-56150 19990922; BR 9914061 A BR 1999-14061 19990922, WO 1999-CH450 19990922; EP 1115949 A1 EP 1999-942696 19990922, WO 1999-CH450 19990922; EP 1233106 A1 Div ex EP 1999-942696 19990922, EP 2002-1228 19990922; AU 754452 B AU 1999-56150 19990922; EP 1115949 B1 EP 1999-942696 19990922, WO 1999-CH450 19990922, Related to EP 2002-1228 19990922; DE 59903926 G DE 1999-503926 19990922, EP 1999-942696 19990922, WO 1999-CH450 19990922
FDT AU 9956150 A Based on WO 200019016; BR 9914061 A Based on WO 200019016; EP 1115949 A1 Based on WO 200019016; EP 1233106 A1 Div ex EP 1115949; AU 754452 B Previous Publ. AU 9956150, Based on WO 200019016; EP 1115949 B1 Related to EP 1233106, Based on WO 200019016; DE 59903926 G Based on EP 1115949, Based on WO 200019016
PRAI CH 1998-1958 19980925
AB WO 200019016 A UPAB: 20000606
NOVELTY - An anti-falsification article (AFA) comprising at least one anti-falsification element (AFE) with at least one photoluminesent segment (PLS) exhibiting linearly polarized photoluminescence and/or linearly polarized absorption is new.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for preparation of an anti-falsification article by providing an object with an AFE having at least one segment exhibiting linear polarized photoluminescence and/or linearly polarized absorption.

USE - The AFA can be used to make falsification of an object very difficult or impossible (claimed), to verify the genuineness or validity of an object (claimed), and to facilitate or simplify its identification (claimed). The AFT is useful for application to groups of banknotes, checks, bonds, shares, identity cards, leadership certificates (sic), admission tickets, stamps, bank cards, and credit cards.

ADVANTAGE - The AFE make falsification of an object very difficult or impossible, and avoid some drawbacks of previous AFE, i.e. difficulty in recognizing authenticity marks and complex equipment required for this, and provides a solution to the problem of the relative simplicity of producing false papers ,etc.

DESCRIPTION OF DRAWING(S) - Figure 3 shows a graphical representation of anti-falsification objects.
paper 1
strips 2
printing 3

strips 4
Dwg.0/3

L116 ANSWER 5 OF 12 WPIX (C) 2003 THOMSON DERWENT
AN 2000-226523 [20] WPIX
DNN N2000-169926
TI Wear block for press tool, has wedge between tapered plates for adjusting thickness of wear block.
DC P52 P71
IN PARKINSON, S; **SMITH, P**
PA (BMCC) ROVER GROUP LTD
CYC 1
PI GB 2342063 A 20000405 (200020)* 15p
ADT GB 2342063 A GB 1998-21093 19980930
PRAI GB 1998-21093 19980930
AB GB 2342063 A UPAB: 20000426
NOVELTY - The press tool has a number of wear blocks (10b) each comprises of two tapered plates (11, 12) and a double-sided wedge (13). Movement of the wedge relative to the wear plates (11, 12) changes the thickness (t) of the wear block and is used to adjust the running clearance between the two **dies** (5) of the press tool.
USE - For press tools.
ADVANTAGE - The expense of replacing wear blocks is avoided.
DESCRIPTION OF DRAWING(S) - The drawing shows part of the press tool including the wear block.
Die 5
Wear block 10b
Tapered plates 11, 12
Wedge 13
Wear block thickness t
Dwg.4/4

L116 ANSWER 6 OF 12 WPIX (C) 2003 THOMSON DERWENT
AN 1996-181378 [19] WPIX
DNN N1996-152415
TI Secure access system e.g. for CATV - has **IC** card reader and writer with two separate and independent card receptacles with **IC** card required for each receptacle to access programs.
DC T04 T05 W02 W03
IN BAR-ON, G; FINK, D; HANDELMAN, D; KRANC, M; **SMITH, P**; ZUCKER, A; KRANTZ, M
PA (NEWS-N) NEWS DATACOM LTD; (NEWS-N) NEWS DATA COM LTD
CYC 22
PI EP 706291 A2 19960410 (199619)* EN 19p
R: AT BE CH DE DK ES FR GB GR IE IT LI LU MC NL PT SE
AU 9533036 A 19960418 (199623)
CA 2159779 A 19960404 (199629)
JP 08214278 A 19960820 (199643) 63p
EP 706291 A3 19970319 (199722)
US 5666412 A 19970909 (199742) 18p
US 5774546 A 19980630 (199833)
IL 111151 A 19980924 (199844)
AU 696725 B 19980917 (199849)
US 5878134 A 19990302 (199916)
EP 706291 B1 20010103 (200102) EN
R: AT BE CH DE DK ES FR GB GR IE IT LI LU MC NL PT SE
ES 2153005 T3 20010216 (200114)
DE 69519782 E 20010208 (200115)
US 6298441 B1 20011002 (200160)
US 2001042049 A1 20011115 (200172)
ADT EP 706291 A2 EP 1995-115554 19951002; AU 9533036 A AU 1995-33036 19951003;

CA 2159779 A CA 1995-2159779 19951003; JP 08214278 A JP 1995-291606 19951003; EP 706291 A3 EP 1995-115554 19951002; US 5666412 A US 1995-375995 19950120; US 5774546 A Div ex US 1995-375995 19950120, US 1997-780501 19970108; IL 111151 A IL 1994-111151 19941003; AU 696725 B AU 1995-33036 19951003; US 5878134 A Cont of US 1995-375995 19950120, US 1997-925547 19970908; EP 706291 B1 EP 1995-115554 19951002; ES 2153005 T3 EP 1995-115554 19951002; DE 69519782 E DE 1995-619782 19951002, EP 1995-115554 19951002; US 6298441 B1 Cont of US 1995-375995 19950120, CIP of US 1997-925547 19970908, US 1998-115489 19980714; US 2001042049 A1 Cont of US 1995-375995 19950120, CIP of US 1997-925547 19970908, Cont of US 1998-115489 19980714, US 2001-827448 20010406

FDT US 5774546 A Div ex US 5666412; AU 696725 B Previous Publ. AU 9533036; US 5878134 A Cont of US 5666412; ES 2153005 T3 Based on EP 706291; DE 69519782 E Based on EP 706291; US 6298441 B1 Cont of US 5666412; US 2001042049 A1 Cont of US 5666412, CIP of US 5878134

PRAI IL 1994-111151 19941003

AB EP 706291 A UPAB: 20011105

The CATV system has a CATV network, and apparatus for transmission over the network information to a number of subscriber units. Each includes a CATV decoder and an **IC** card reader and writer, coupled to the decoder.

Two separate **IC** card receptacles are used. **IC** cards are inserted into the two separate receptacles and are separately accessed by the **IC** card reader and writer.

USE/ADVANTAGE - E.g. **IC** card billing for pay television, telephone systems, electronic mail, audio programs etc. Increased security and flexibility. Allows parental control over viewing.

Dwg.1/8

L116 ANSWER 7 OF 12 WPIX (C) 2003 THOMSON DERWENT

AN 1995-036511 [05] WPIX

DNN N1995-028701 DNC C1995-016445

TI Hypereutectic aluminium -silicon alloy prepd. by powder sintering - with facilitated compaction and reduced galling, for wear-resistant and structural applications.

DC M22 M26 P53

IN MAHMOUD, M S; PURNELL, C G; **SMITH, P**; MAHMOUD, M

PA (ALUM-N) ALUMINIUM POWDER CO LTD; (BRIC-N) BRICO ENG LTD

CYC 19

PI WO 9429489 A1 19941222 (199505)* EN 25p
RW: AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE
W: GB JP KR US
GB 2294475 A 19960501 (199621) 1p
EP 746633 A1 19961211 (199703) EN
R: DE ES FR IT
US 5613184 A 19970318 (199717) 8p
GB 2294475 B 19970416 (199719)
EP 746633 B1 19980826 (199838) EN
R: DE ES FR IT
DE 69412862 E 19981001 (199845)
ES 2119199 T3 19981001 (199848)

ADT WO 9429489 A1 WO 1994-GB1180 19940531; GB 2294475 A WO 1994-GB1180 19940531, GB 1995-24030 19951123; EP 746633 A1 EP 1994-916337 19940531, WO 1994-GB1180 19940531; US 5613184 A WO 1994-GB1180 19940531, US 1995-553712 19951130; GB 2294475 B WO 1994-GB1180 19940531, GB 1995-24030 19951123; EP 746633 B1 EP 1994-916337 19940531, WO 1994-GB1180 19940531; DE 69412862 E DE 1994-612862 19940531, EP 1994-916337 19940531, WO 1994-GB1180 19940531; ES 2119199 T3 EP 1994-916337 19940531

FDT GB 2294475 A Based on WO 9429489; EP 746633 A1 Based on WO 9429489; US 5613184 A Based on WO 9429489; GB 2294475 B Based on WO 9429489; EP 746633 B1 Based on WO 9429489; DE 69412862 E Based on EP 746633, Based on WO

9429489; ES 2119199 T3 Based on EP 746633
PRAI GB 1993-11618 19930604; GB 1995-24030 19951123
AB WO 9429489 A UPAB: 19950207
An Al alloy prepd. by powder metallurgy has a structure comprising at least two interpenetrating reticular structure derived from the original powder particles. These include a near-eutectic Al-Si based material and a hypereutectic Al-Si based material. The two powders are mixed, compacted and sintered.
USE - The Al-Si alloy, having an overall hypereutectic compsn. is suitable for wear-resistant and structural applications.
ADVANTAGE - The powder metallurgical route enables near net-shape compaction and sintering. The high Si level facilitates compaction and lessens galling of the compaction **die**.
Dwg.1/7

L116 ANSWER 8 OF 12 WPIX (C) 2003 THOMSON DERWENT
AN 1993-345594 [44] WPIX
TI Material characteristic scanner appts. for textiles - has specimen load scanner, width scanner, and deformation scanner, all coupled via A-D converters to **integrated circuit** input. NoAbstract..
DC S03 X25
IN JIRSAK, O; LUKAS, D; MACEK, P; **SMITH, P**
PA (JIRS-I) JIRSAK O
CYC 1
PI CS 9200314 A2 19930811 (199344)* 1p
ADT CS 9200314 A2 CS 1992-314 19920205
PRAI CS 1992-314 19920205
AB CS 9200314 A UPAB: 19931213
Dwg.0/0

L116 ANSWER 9 OF 12 WPIX (C) 2003 THOMSON DERWENT
AN 1990-187638 [25] WPIX
DNN N1990-145926
TI Automatic water delivery system for saunas - has timer control to activate valve and deliver measure of water from reusable plastic reservoir via pipe.
DC P33 X27
IN HEDGES, R T; **SMITH, P**
PA (HEDG-I) HEDGES R T; (SMIT-I) SMITH P
CYC 1
PI GB 2225939 A 19900620 (199025)*
GB 2225939 B 19930526 (199321)
ADT GB 2225939 A GB 1988-29290 19881215; GB 2225939 B GB 1988-29290 19881215
PRAI GB 1988-29290 19881215
AB GB 2225939 A UPAB: 19930928
The water delivering system has a removeable, self sealing and reusable plastic reservoir (4) located on the system. A variable, electronic timer control (6) activates an electromechanical valve (5). This delivers a measure of water from the reservoir at a pre-selected time interval. The outflowing water is piped down to discharge.
A push-button control permits the user to bypass the timer. This control will deliver an instant stream of water for as long as the button is depressed. The system utilises low voltage **micro-chip** technology and battery power.
USE/ADVANTAGE - Delivery of water onto hot stones in sauna. Safe, self contained, simple installation.
2/3

L116 ANSWER 10 OF 12 JAPIO COPYRIGHT 2003 JPO
AN 2000-323436 JAPIO
TI METHOD FOR FORMING BARRIER LAYER FOR USE IN COPPER INTERCONNECTION METHOD

IN DENNING DEAN J; GARCIA SAM S; **SMITH** BRADLEY **P**; LOOP DANIEL J; HAMILTON GREGORY NORMAN; ISLAM MOHAMMED RABIUL; BRIAN G ANTHONY
PA MOTOROLA INC
PI JP 2000323436 A 20001124 Heisei
AI JP 2000-51583 (JP2000051583 Heisei) 20000228
PRAI US 1999-261879 19990302
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2000
AB PROBLEM TO BE SOLVED: To manufacture a great amount of copper interconnection parts at lower costs, and enhance yield and reliability by a method wherein power for both a sputtering target and a coil is controlled between the stacks of barrier layers.
SOLUTION: After a **wafer** is disposed in a chamber 40 and the chamber is stabilized, power of, for example, 1000 W is applied on a target 48, and this power is continuously applied between the stacks of barrier layers. First, power of, for example, about 1000 W is supplied to the target 48, and substantially simultaneously power of, for example, about 1500 W is supplied to a coil 52. Namely, an initial part of the barrier film is deposited between high coil powering sequences, and the other part of the barrier film is deposited between low coil power or zero coil powering sequences. Accordingly, the power to the coil is selectively controlled between the stacks of the barrier film, whereby it is possible to design the stress of the barrier film in accordance with each stress of upside and downside layers.

L116 ANSWER 11 OF 12 JAPIO
AN 1999-154457 JAPIO
TI CARD ASSEMBLY
IN **BOJKOV CHRISTO**; FINK RICHARD; KUMAR NALIN; TIKHONSKI ALEXEI; YANIV ZVI
PA NOMURA TRADING CO LTD
SI DIAMOND TECHNOL INC
PI JP 11154457 A 19990608 Heisei
AI JP 1998-279262 (JP10279262 Heisei) 19980826
PRAI US 1997-920011 19970826
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1999
AB PROBLEM TO BE SOLVED: To produce a mechanism requiring no use of a **microelectronics** process by arranging a base board and plural electrically conductive stripes to cover the base board, and forming a diamond layer on the base board exposed between it and the electrically conductive stripes.
SOLUTION: A diamond layer is desirably a CVD diamond or an amorphous diamond. A cathode composed of a base board 1101 and a metallic wire 1102 is put in an alcohol solution put in a vessel filled with an electrolytic solution such as Al(NO<SB>3</SB>)<SB>3</SB> and Mg(NO<SB>3</SB>)<SB>2</SB>. A substance such as Ni, SUS and Pt can be used as an anode. When negative voltage is impressed on the anode, diamond particles 1701 of the nanosize are accumulated on the metallic wire 1102 to become a nucleus of diamond growth. A diamond layer is formed by performing chemical vapor deposition(CVD) of diamond by putting this cathode structure in a vacuum device.

L116 ANSWER 12 OF 12 JAPIO
AN 1998-092921 JAPIO
TI **INTEGRATED CIRCUIT** HAVING DUMMY STRUCTURES AND METHOD OF FORMING THE SAME
IN GILBERT PERCY V; IYER SUBRAMONEY; **SMITH** BRADLEY **P**; THOMPSON MATTHEW A; KEMP KEVIN; DHAR RAJIVE
PA MOTOROLA INC
PI JP 10092921 A 19980410 Heisei

AI JP 1997-237832 (JP09237832 Heisei) 19970820
PRAI US 1996-704481 19960821
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1998

AB PROBLEM TO BE SOLVED: To form a structure which improves the flatness of the polishing process, without adding any manufacturing step, as dishing is caused by the change of the polishing rate due to the pattern density variation if dummy structures are positioned at random during polishing a nonconductive material for filling up trench structures at a semiconductor device manufacturing process having a trench isolation.
SOLUTION: Dummy structures 20 are disposed on first parts not occupied by active devices so that the occupied density of the first parts is equal to second parts occupied by active devices, thus make the polishing rate uniform over the surface of a semiconductor substrate. A dummy substrate pattern is added to a layout pattern of an **integrated circuit** and can be determined previously so as to avoid intersection of well boundaries or active regions 27 and avoid the existence below conductive materials such as polysilicon layers or interconnect structures, without adding a manufacturing step.